THE UNIVERSITY OF TEXAS AT AUSTIN Date: 9/4/13

RECOMMENDATION FOR CHANGE IN ACADEMIC RANK/STATUS

Name: Andreas Gerstlauer Present Rank: Assistant Professor

Years of Academic Service *(Include AY 2013-14 in each count)*:

At UT Austin since: 9/1/08 (m/d/y) In present rank: 6 (# of years); In Probationary Status (TT **only**): 6 (# of years)

Department: Electrical and Computer Engineering

Other: _____

College/School: Cockrell School of Engineering

Recommended action[1]:

By Budget Council/Executive Committee: Promote to Associate Professor

Vote[2] for promotion 26; Against 0; Abstain 0; Absent 8

By Department Chair: Promote to Associate Professor

By SBS Executive Committee: _____

Vote[2] for promotion _____; Against _____; Abstain _____; Absent _____

By Director: _____

By College/School Advisory Committee: Promote

Vote[2] for promotion 7; Against 0; Abstain 0; Absent 0

By Dean: Promote

Administrative Action: Promote to Associate Professor

Date Action Effective: September 1, 2014
(To be submitted to the Board of Regents as part of the annual budget.)

By: _____ Date: 12/16/2013
For the President

[1]See "Chart of Recommended Actions" for eligible recommended actions applicable to specific conditions and administrative levels.

[2]All votes are to be recorded as For, Against, or Abstain. (Note: unexplained abstentions will be interpreted as weak negative votes by the President's Committee.) Also record number of absent eligible voting members.

EVPP/4.13

EXHIBIT
P's 173

Dean's Assessment
Andreas Gerstlauer
Department of Electrical and Computer Engineering

Andreas Gerstlauer received his Vordiplom (BS) and Dipl-Ing (MS) in Electrical Engineering from the University of Stuttgart, Germany in 1991 and 1997, respectively, and an MS and Ph.D. in Information and Computer Science from the University of California, Irvine in 1998 and 2004, respectively. He continued at UC Irvine as an assistant researcher until he was appointed an assistant professor at UT Austin in 2008.

Ten external letters were submitted as part of the promotion dossier, five were suggested by the candidate and five were selected by the budget council. Eight reviewers are faculty at US universities, one is a faculty member at a European university, and one is a senior technical staff member in industry. One reviewer is a member of NAE.

Teaching
Dr. Gerstlauer has taught one undergraduate course and two graduate courses: EE 319K, *Introduction to Embedded Systems* (four times); EE 382V *Embedded System Design and Modeling* (four times); and EE 382V *System on a Chip* (three times). His average overall instructor/course ratings for these courses are 4.05/3.78, 4.20/3.55, and 4.33/3.87 respectively. Dr. Gerstlauer's ratings compare favorably with the weighted average/median instructor ratings for assistant professors in the Department of Electrical and Computer Engineering over the last five years (4.06/4.08 for undergraduate courses) and (4.22/4.36 for graduate courses).

In collaboration with Professors Yerraballi and Valvano, Dr. Gerstlauer is developing a massively open online course (MOOC) based on EE 319K. This course will be delivered through the edX consortium during the 2014 spring semester and will include a physical hardware laboratory component. This is believed to be the first time that a MOOC will include a laboratory component using physical hardware, as opposed to simulations of hardware.

Research
Dr. Gerstlauer's research is in the area of system-level design of embedded computer systems, with a focus on design automation methodologies, technologies and tools. His primary focus has been on tools for modeling systems-on-a-chip that are embedded in a variety of products, from consumer electronics to civilian spacecraft and military systems. Dr. Gerstlauer's methods and tools provide assistance for teams of designers in making key decisions and automating the design of the entire computing system based on the design decisions.

At UT, Dr. Gerstlauer has published nine archival journal papers (eight in print and one accepted), 32 peer-reviewed conference papers (these conferences have acceptance rates in the range of 17 to 34%). His career totals are 12 archival journal papers, 54 peer-reviewed conference papers, and three co-authored books.

Dr. Gerstlauer's extramural research funding in rank includes nine grants and four gifts, totaling nearly $2.2 million (his share is $1.4 million). The research grants have been funded by federal agencies (National Science Foundation, DARPA, and Army Research Office) and industrial groups (Semiconductor Research Corporation, Samsung). He is the principal investigator on ten of these research grants/gifts.

The letters from external reviewers are consistently strong. Dr. Gerstlauer's specific contributions to the field and the impact of his work are well documented.

Dr. Arvind (Massachusetts Institute of Technology, NAE) writes, "There is a good balance between *tools* versus *design* papers. For me Andreas['] work would lack credibility without the design papers. The topics covered by these papers are of central concern in ESL [embedded computer systems]. I also found the architecture modeling paper and the OS paper together offering some creative insights in a difficult modeling question."

Dr. Nikil Dutt (University of California, Irvine) writes, "After joining UT Austin, Dr. Gerstlauer has continued to build on this momentum by creating abstractions for RTOS modeling for heterogeneous multi-core platforms, hardware-dependent software design methodologies, and transaction-level modeling for efficient exploration of communication architectures. His recent work on speeding up system-level simulation and embedded software modeling already show early signs of impact both in the research arena, as well as for industrial practitioners."

Dr. Milos Ercegovac (University of California, Los Angeles) writes, "These works are typical of his research: there is a clear, original idea, a good technical depth, and strong experimental results. Prof. Gerstlauer and his collaborators made notable contributions in identifying key principles of electronic system design, covering both hardware and software aspects."

Dr. Peter Hofstee (IBM Austin Research Laboratory) writes, "... what most impresses me about Dr. Gerstlauer's work, is on the one hand a rigorous drive for the abstraction and elegance one expects of academic research with lasting value, and at the same time a high degree of completeness and realism that allows his research to be readily applicable. It is unusual to see this span of interest and capability within a single researcher."

Dr. Martin Wong (University of Illinois at Urbana-Champaign) writes, "... Andreas has established a diverse and high-quality research program that is certainly on par with if not better than any of his peers'." "... Andreas is highly visible, well known and respected in the broader automation community."

Advising and Student Mentoring

At UT Austin, Dr. Gerstlauer has graduated three co-supervised PhD students, three MS thesis students (one was co-supervised), and five MS report students. He is currently supervising or co-supervising seven PhD students and two MS students. He has also served as the faculty advisor to several upper-division undergraduate students in Computer Engineering and Embedded Systems tracks.

University Service

Dr. Gerstlauer has served on several committees within the Department of Electrical and Computer Engineering. He has been actively engaged with the undergraduate curricula and with graduate student recruiting and admissions. He also served on the faculty search committee one year.

Professional Service

Dr. Gerstlauer is an associate editor for *Transactions on Embedded Computing Systems* within the Association for Computing Machinery (ACM) and he serves on the editorial board for *Design Automation for Embedded Systems* (SpringerLink). He has also served on the technical program committee for several technical conferences.

Other Evidence of Merit or Recognition

In 2013, Dr. Gerstlauer's work with graduate student Ardavan Pedram was recognized with the Best Poster Award by the IEEE Computer Society Technical Committee on Parallel Processing at an international PhD forum on parallel and distributed processing.

Overall Assessment

Dr. Gerstlauer has developed a strong research program with a high level of publication productivity; he has secured a sustainable level of research funding from federal and corporate sources; and the quality and impact of his research are highly regarded by the external reviewers. His teaching contributions at the undergraduate and graduate level are strong.

Accordingly, I recommend promotion of Andreas Gerstlauer to associate professor with tenure.

Sharon L. Wood, Interim Dean
2 November 2013

COCKRELL SCHOOL OF ENGINEERING
THE UNIVERSITY OF TEXAS AT AUSTIN

Department of Electrical and Computer Engineering • Engineering Science Building
1 University Station C0803 • Austin, Texas 78712-0240 • (512) 471-6179 • Fax (512) 471-3652

September 30, 2013

Chair's letter in support of the promotion of Prof. Andreas Gerstlauer to the rank of associate professor with tenure

Prof. Gerstlauer joined the Department of Electrical and Computer Engineering in September 2008. He made seminal contributions to embedded systems and electronic system-level design automation before coming to UT and while at UT. The Budget Council recognized his strong accomplishments and determined that he meets all expectations for promotion at the premier departments of Electrical and Computer Engineering in the nation by a vote of 26 YES, 0 NO and 0 ABSTAIN. Our associate professors voted 7 YES, 0 NO and 0 ABSTAIN in support of promotion.

Teaching

Prof. Gerstlauer is a strong teacher with average instructor scores in a required undergraduate class that he has regularly taught ranging from 3.7 to 4.3 and average instructor scores in graduate courses ranging from 3.8 to 4.6. His 3.7 instructor score in EE319K is an aberration due to the use of electronic evaluations that semester. All other course instructor surveys used paper forms. Both his peers and students rate him as an excellent instructor who has mastered the use of the blackboard and technology to explain difficult concepts.

Beyond the classroom teaching, Andreas is truly a leader and innovator in education within our department. Andreas completely revamped our "System-on-Chip (SoC) Design" class. More significantly, he has developed a graduate class on "Embedded System Design and Modeling." The class was very well received by our students, as evidenced by an enrollment of close to 20 students in its first and subsequent offerings. The class is unique in that five final projects by student teams in the class have led to publications in international conference proceedings. The teaching material that he developed for this class is in use at several universities worldwide, including Northeastern University, Iowa State University, Istanbul Technical University, Turkey, the Federal University of Pernambuco, Brazil, the University of Teheran, Iran, and the Universities of Oldenburg and Stuttgart in Germany.

Andreas is also part of a team that is turning EE319K into a massively open online course (MOOC) class to be offered by edX in Spring 2014. To my knowledge, this is the first MOOC class that will have a physical hardware laboratory as opposed to a virtual laboratory.

Research

Andreas' work is characterized by its rigor and emphasis on building prototypes that demonstrate the impact of his discoveries. He has made seminal contributions to formalizing system-level

specifications and the development of tools for the co-design of hardware and software that meet these specifications while meeting performance, power consumption and reliability goals. Most importantly, his work provides designers with an ability to trade power consumption, performance and reliability adaptively, depending on the current application running on the embedded system. Prof. Dutt (UC Irvine) notes that Andreas "is the key intellectual contributor behind the SpecC modeling language and methodology, which (besides the high citation counts) led to development of semantics for the SystemC language, which is now the default industry standard specification language for mixed hardware/software design implementations." His work at UT on creating abstractions for modeling heterogeneous multi-core platforms, system-level simulation and embedded software modeling, transaction-level modeling for efficient exploration of communication architectures and hardware-dependent software design has received considerable attention in the literature and is starting to have an impact on industrial design. Dr. Hofstee (IBM) states that Andreas' work to date is the "type of work that those of us who have to bridge between academia and commercial practice look for." At a very recent meeting with Greg Delagi, senior vice president and general manager of Embedded Processing at Texas Instruments, that Andreas and I attended, Greg declared that Andreas' research and inventions is what is needed to enable progress in the next generation of embedded systems and controllers.

As an example of the high quality of Andreas' work, I note that he demonstrated in the past couple of years that modeling preemptive behavior in discrete timing simulations can lead to potentially unbounded timing errors. He developed an integrated modeling approach to automatically and optimally adjust timing granularities and remove the sources of timing errors. The work also provides designers with an ability to navigate fundamental speed and accuracy tradeoffs. His 2012 *IEEE Embedded System Letters* paper on this topic was among the top-five accessed articles in April, August and November 2012.

More recently, Andreas has been collaborating with other researchers at UT to make key contributions to new areas. He has been working with Prof. Michael Orshansky on approximate logic synthesis and on error-tolerant circuits for signal processing. As I noted in the letter I wrote for Michael, this work has attracted a lot of attention in academic and industrial circles, despite the fact that it is very recent. Prof. Ercegovac (UCLA) states that "This work has also attracted attention from IBM and AMD as well as Stanford and University of Wisconsin," and "These works are typical of his research: there is a clear, original idea, a good technical depth, and strong experimental results." His recent work with Prof. Robert van de Geijn (UT CS) on the co-design of algorithms and architectures for a novel linear algebra processor achieved orders of magnitude better efficiency (as measured in energy per operation) than any currently known linear algebra processor architecture.

Prof. Gerstlauer is very well funded by highly competitive peer-reviewed grants from NSF, SRC and DOD. He is also well funded by industry, yet another recognition of the impact that his work has had on commercial practice. Indeed, he has been awarded more than enough research funding to create and sustain a world-class research group.

Our department has adopted the practice of comparing each colleague with his or her most prominent peers at the first tier departments in Electrical and Computer Engineering, such as MIT, Stanford, the University of California Berkeley, the University of Illinois Urbana Champaign (UIUC), Georgia Tech, Caltech and Princeton. In consultation with Andreas and senior professors in the area in our department, I selected Profs. Valeria Bertacco (who was promoted to associate professor at Michigan in 2009), Luca Carloni (who was promoted to associate professor at Columbia in 2009) and Sanjit Seshia (who was promoted to associate professor at UC Berkeley in 2011). The comparison shows that Andreas is as productive as his

peers at the time of promotion in terms of journal publications and publications in top-tier conferences. His current H index is comparable to Bertacco and Seshia but lower than that of Carloni who is more senior. Prof. Henkel (Karlsruhe Institute of Technology) supports my conclusion and provides an excellent summary of the letters of reference when he states that "Dr. Gerstlauer is a top young researcher. He has shown excellent research capabilities in the past and I believe that he has a great academic research career in front of him. I believe that any EE, CS, ECE departments with world rank would be delighted to hire him." Confirming this opinion, Prof. Wong (UIUC) writes "Andreas has an outstanding research, teaching and service record, and we would be glad to have him on our faculty here at UIUC."

Service

Andreas has provided excellent service to both UT and the profession. Details can be found in his resume and the budget council statement.

Summary

Andreas is a strong and innovative teacher and, in my opinion, a rising international star in embedded systems and electronic system-level design automation who brings to the field a unique mix of academic rigor and practical impact. He has served UT and his profession well. I strongly endorse his promotion to associate professor with tenure.

Sincerely,

Prof. Ahmed H. Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering

THE UNIVERSITY OF TEXAS AT AUSTIN
Cockrell School of Engineering
Standard Resume

FULL NAME: Andreas Gerstlauer **TITLE:** Assistant Professor

DEPARTMENT: Electrical and Computer Engineering

EDUCATION:

University of California, Irvine	Information & Computer Science	Ph.D.	4 / 2004
University of California, Irvine	Information & Computer Science	M.S.	9 / 1998
University of Stuttgart, Germany	Electrical Engineering	Dipl.-Ing. (M.S.)	5 / 1997
University of Stuttgart, Germany	Electrical Engineering	Vordiplom (B.S.)	10 / 1991

PROFESSIONAL REGISTRATION: None

CURRENT AND PREVIOUS ACADEMIC POSITIONS:

University of Texas at Austin	Assistant Professor	Fall 2008-present
University of California, Irvine	Assistant Researcher	Summer 2004-Summer 2008
University of California, Irvine	Research & Teaching Assistant	Fall 1997-Spring 2004
University of Stuttgart, Germany	Research Assistant	Fall 1993-Spring 1997

OTHER PROFESSIONAL EXPERIENCE:

Ehrler Prüftechnik, Germany	Senior Eng. & Proj. Manager	Aug. 1989-Mar. 1997
Hewlett Packard GmbH, Germany	Intern	Jun. 1994-Aug.1994

CONSULTING:

None

HONORS AND AWARDS:

IEEE Computer Society Technical Committee on Parallel Processing	Best Poster Award for student Ardavan Pedram at the International Parallel & Distributed Processing Symposium (IPDPS) Ph.D. forum	2013
IEEE	Senior Member	2011
Advanced Micro Devices, Inc.	AMD Chair in Computer Engineering	2010-present
Design, Automation and Test in Europe Conference	OS Modeling Paper Selected as One of the Most Influential Contributions in 10 Years	2008
Design Automation Conference	Young Student Mentor	2002
Motorola, Inc.	Motorola Research Fellow	2000-2001
Design Automation Conference	Professional Development Award	1998
University of Stuttgart, Germany	Graduated *summa cum laude* *("mit Auszeichnung")*	1997

MEMBERSHIPS IN PROFESSIONAL AND HONORARY SOCIETIES:

IEEE Circuits and Systems Society	1997-present
IEEE Computer Society	1997-present
ACM Special Interest Group on Design Automation (SIGDA)	1997-present

UNIVERSITY COMMITTEE ASSIGNMENTS:

Departmental

- Member, Faculty Search Committee, Electrical and Computer Engineering	2010
- Member, Steering Committee, Wireless Networking and Communications Group (WNCG)	2010-present
- Coordinator, Graduate Student Site Visit, Integrated Circuits and Systems (ICS) Track, Electrical and Computer Engineering	2009-present
- Member, Steering Committee, Computer Engineering Research Center (CERC)	2008-2013
- Member, Graduate Admissions Committee, Integrated Circuits and Systems (ICS) Track, Electrical and Computer Engineering	2008-present
- Member, Graduate Admissions Committee, Computer Engineering (CE)/Computer Architecture and Embedded Processors (CAEP)Track, Electrical and Computer Engineering	2008-present
- Member, Curriculum Committee, Integrated Circuits and Systems (ICS) Track, Electrical and Computer Engineering	2008-present
- Member, Curriculum Committee, Computer Engineering (CE)/Computer Architecture and Embedded Processors (CAEP) Track, Electrical and Computer Engineering	2008-present
- Member, Graduate Studies Committee, Electrical and Computer Engineering	2008-present

PROFESSIONAL OUTSIDE COMMITTEES:

Governmental

- Panel Reviewer, National Science Foundation	2013

Journals

- Associate Editor, ACM Transactions on Embedded Computing Systems (TECS)	2013-present
- Editorial Board, Design Automation for Embedded Systems (DAEM)	2012-present

Conferences

- Chair, Technical Area “Architecture and Implementation,” Asilomar Conference on Systems, Signals and Computers (ACSSC)	2013
- Co-Chair (with J. Xue), Track T8 “Embedded Systems/HW-SW Codesign/Logic & High Level Synthesis,” IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)	2013
- Co-Chair (with M. Kreutz), Technical Program Committee, Electronic System Level Synthesis Conference (ESLsyn)	2013
- Chair, Subcommittee “EDA1: System-Level Design and Codesign,” ACM/EDAC/IEEE Design Automation Conference (DAC)	2012-2013
- Member, Technical Program Committee, Electronic System Level Synthesis Conference (ESLsyn)	2012
- Co-Chair (with P. Brisk), Track T11 “Logic and high-level synthesis, SW synthesis, HW-SW co-design,” IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)	2012

- Co-Organizer (with C. Haubelt), Special session on "Embedded Multi-Processor Software Synthesis," ACM/EDAC/IEEE Design Automation Conference (DAC) 2011
- Registration Chair, IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) 2011
- Member, Technical Program Committee, IEEE International Conference on Computer Design (ICCD) 2010-2013
- Co-organizer (with C. Haubelt), Workshop on Compiler-Assisted System-On-Chip Assembly (CASA) 2010
- Co-Organizer (with R. Dömer), Designer Forum session on "Embedded Software Development for Multi-Processor System-on-Chip," IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC) 2010
- Member, Technical Program Committee, IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), Work-in-Progress (WiP) Track 2010
- Chair, Technical Program Committee (TPC), Austin Conference on Integrated Systems and Circuits (ACISC) 2010
- Chair, Topic "Hardware/Software Codesign," IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) 2009-2010
- Tutorial Chair, Austin Conference on Integrated Systems and Circuits (ACISC) 2009
- Member, Technical Program Committee, Austin Conference on Integrated Systems and Circuits (ACISC) 2009
- Co-Organizer (with R. Dömer, W. Mueller), Special session on "Hardware Dependent Software for Multi-Core Embedded Systems," IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC) 2009
- Member, Technical Program Committee, IEEE/ACM/IFIP International Conference on Hardware/Software Co-Design and System Synthesis (CODES+ISSS) 2009-2013
- Member, Technical Program Committee, International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES) 2009, 2011
- Member, Technical Program Committee, International Conference on Embedded Systems and Critical Applications (ICESCA) 2008
- Member, Technical Program Committee, International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS) 2008-2010
- Local Arrangements Chair, International Embedded Systems Symposium (IESS) 2007
- Member, Technical Program Committee, International Embedded Systems Symposium (IESS) 2007-2013
- Member, Technical Program Committee, Design, Automation and Test in Europe (DATE) Conference 2006-2013

COMMUNITY ACTIVITIES:

Reviewer

- IEEE Micro 2013
- Elsevier Embedded Hardware Design (Microprocessors and Microsystems) 2012
- IEEE Computer Architecture Letters (CAL) 2012
- IEEE Transactions on Multimedia (TMM) 2012
- ACM Journal of Emerging Technologies in Computing (JETC) 2011
- IEEE Embedded System Letters (ESL) 2009-2010
- IEEE Transactions on Industrial Informatics (TII) 2009-2010
- ACM Transactions on Embedded Computing Systems (TECS) 2009-2013

- ACM Transactions on Design Automation of Electronic Systems (TODAES)	2008-2013
- EURASIP Journal of Embedded Systems (JES)	2007
- Design Automation for Embedded Systems (DAEM) Journal	2006, 2012
- Journal of Systems Architecture (JSA)	2005, 2010
- ACM/IEEE Design Automation Conference (DAC)	1998-2011
- IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)	2003-2004, 2009-2010
- IEEE/ACM/IFIP International Conference on Hardware/Software Co-design and System Synthesis (CODES+ISSS)	2003-2004
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)	2002-2003
- Journal for Circuits, Systems and Computers (JCSC)	2002
- Design, Automation and Test in Europe (DATE) Conference	1999, 2002
- IEEE Transaction on VLSI Systems (TVLSI)	2000, 2005
- IEEE Design & Test of Computers (D&T) Magazine	1999, 2010
- International Symposium on System Synthesis (ISSS)	1998

Conferences

- Session Chair, ACM/EDAC/IEEE Design Automation Conference (DAC)	2011
- Session Chair, International Embedded Systems Symposium (IESS)	2009
- Session Co-Chair, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)	2009
- Session Chair, "Automating Model Generation and Implementation," Design, Automation and Test in Europe (DATE) Conference	2009
- Session Chair, International Embedded Systems Symposium (IESS)	2007
- Organizer Center for Embedded Computer Systems (CECS) booth, ACM/IEEE Design Automation Conference (DAC)	2007
- Session Co-Chair, Design, Automation and Test in Europe (DATE) Conference	2006

PUBLICATIONS (titles are embedded hyperlinks):

A. Refereed Archival Journal Publications

J12. D. Pfeifer, J. Valvano, A. Gerstlauer, "SimConnect and SimTalk for Distributed Cyber-Physical System Simulation," *Simulation: Transactions of the Society for Modeling and Simulation International*, accepted for publication, November 2012.

J11. K. He, A. Gerstlauer, M. Orshansky, "Circuit-Level Timing-Error Acceptance for Design of Energy-Efficient DCT/IDCT-based Systems," *IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)*, vol. 23, no. 6, pp. 961-974, June 2013

J10. J. Lin, A. Gerstlauer, B. L. Evans, "Communication-Aware Heterogeneous Multiprocessor Mapping for Real-Time Streaming Systems," *Journal of Signal Processing Systems*, vol. 69, no. 3, pp. 279-291, December 2012.

J9. A. Pedram, R. A. van de Geijn, A. Gerstlauer, "Codesign Tradeoffs for High-Performance, Low-Power Linear Algebra Architectures," *IEEE Transactions on Computers (TC)*, special issue on Energy Efficient Computing, vol. 61, no. 12, pp. 1724-1736, December 2012. (18% acceptance rate)

J8. P. Razaghi, A. Gerstlauer, "Predictive OS Modeling for Host-Compiled Simulation of Periodic Real-Time Task Sets," *IEEE Embedded System Letters*, vol. 4, no. 1, pp. 5-8, March 2012.

J7. J. Gladigau, A. Gerstlauer, C. Haubelt, M. Streubühr, J. Teich, "Automatic System-Level Synthesis: From Formal Application Models to Generic Bus-Based MPSoCs," *Transactions on*

High-Performance Embedded Architectures and Compilers (Transactions on HiPEAC), vol. 5, no. 4, 22 pages, 2011.

J6. G. Schirner, A. Gerstlauer, R. Dömer, "Fast and Accurate Processor Models for Efficient MPSoC Design," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 15, no. 2, article no. 10, pp. 1-26, February 2010.

J5. A. Gerstlauer, C. Haubelt, A. D. Pimentel, T. P. Stefanov, D. D. Gajski, J. Teich, "Electronic System-Level Synthesis Methodologies," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 28, no. 10, pp. 1517-1530, October 2009.

J4. R. Dömer, A. Gerstlauer, J. Peng, D. Shin, L. Cai, H. Yu, S. Abdi, D. D. Gajski, "System-on-Chip Environment: A SpecC-based Framework for Heterogeneous MPSoC Design," *EURASIP Journal on Embedded Systems (JES)*, vol. 2008, Article ID 647953, 13 pages, 2008.

J3. D. Shin, A. Gerstlauer, R. Dömer, D. D. Gajski, "An Interactive Design Environment for C-Based High-level Synthesis of RTL Processors," *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 16, no. 4, pp. 466-475, April 2008.

J2. A. Gerstlauer, D. Shin, J. Peng, R. Dömer, D. D. Gajski, "Automatic, Layer-based Generation of System-On-Chip Bus Communication Models," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 26, no. 9, pp. 1676-1687, September 2007.

J1. S. B. Saoud, A. Gerstlauer, D. D. Gajski, "Codesign Methodology of Real-Time Embedded Controllers for Electromechanical Systems," *American Journal of Applied Sciences*, vol. 2, no. 9, pp. 1331-1336, October 2005.

B. Refereed Conference Proceedings

C54. J. Miao, A. Gerstlauer, M. Orshansky, "Approximate Logic Synthesis under General Error Magnitude and Frequency Constraints," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, November 2013. (26% acceptance rate)

C53. S. Lee, A. Gerstlauer, "Fine Grain Word Length Optimization for Dynamic Precision Scaling in DSP Systems," *Proceedings of the IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Istanbul, Turkey, November 2013. (20% acceptance rate, 28% incl. short papers)

C52. S. Chakravarty, Z. Zhao, A. Gerstlauer, "Automated, Retargetable Back-Annotation for Host Compiled Performance and Power Modeling," *Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Montreal, Canada, October 2013. (28% acceptance rate)

C51. A. Mariano, D. Lee, A. Gerstlauer, D. Chiou, "Hardware and Software Implementations of Prim's Algorithm for Efficient Minimum Spanning Tree Computation," *Embedded Systems: Design, Analysis and Verification*, Proceedings of the IFIP International Embedded Systems Symposium (IESS), Paderborn, Germany, edited by Gunar Schirner, Marcelo Götz, Achim Rettberg, Mauro C. Zanella, Franz J. Rammig, vol. 403 of IFIP Advances in Information and Communication Technology, Springer, ISBN 978-3-642-38852-1, pp. 151-158, June 2013.

C50. H. Park, A. Gerstlauer, "Toward a Fast Stochastic Simulation Processor for Biochemical Reaction Networks," *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP)*, Washington, DC, pp. 50-58, June 2013. (22% acceptance rate, 36% incl. short papers)

C49. A. Pedram, J. McCalpin, A. Gerstlauer, "Transforming A Linear Algebra Core to An FFT Accelerator," *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP)*, Washington, DC, pp. 175-184, June 2013. (22% acceptance rate, 36% incl. short papers)

C48. P. Razaghi, A. Gerstlauer, "Multi-Core Cache Hierarchy Modeling for Host-Compiled Performance Simulation," *Proceedings of the Electronic System Level Synthesis Conference (ESLSyn)*, Austin, TX, 6 pages, June 2013. (38% acceptance rate)

C47. D. Pfeifer, A. Gerstlauer, J. Valvano, "Dynamic Resolution in Distributed Cyber-Physical System Simulation," *Proceedings of the ACM SIGSIM Conference on Principles of Advanced Discrete Simulation (PADS)*, Montreal, Canada, pp. 277-284, May 2013. (39% acceptance rate)

C46. A. Pedram, A. Gerstlauer, R. van de Geijn, "Floating Point Architecture Extensions for Optimized Matrix Factorization," *Proceedings of the 21st IEEE International Symposium on Computer Arithmetic (ARITH21)*, Austin, TX, pp. 49-58, April 2013. (28% acceptance rate)

C45. K. He, A. Gerstlauer, M. Orshansky, "Low-Energy Digital Filter Design Based on Controlled Timing Error Acceptance," *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, San Jose, CA, pp. 151-157, March 2013.

C44. J. Miao, K. He, A. Gerstlauer, M. Orshansky, "Modeling and Synthesis of Quality-Energy Optimal Approximate Adders," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, pp. 728-735, November 2012. (24% acceptance rate)

C43. J. W. Massey, J. Starr, S. Lee, D. Lee, A. Gerstlauer, R. W. Heath, "Implementation of a Real-Time Wireless Interference Alignment Network," *Proceedings of the Asilomar Conference on Signals, Systems and Computers (ACSSC)*, Pacific Grove, CA, pp. 104-108, November 2012. (invited paper)

C42. D. Lee, H. Park, A. Gerstlauer, "Synthesis of Optimized Hardware Transactors from Abstract Communication Specifications," *Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Tampere, Finland, pp. 403-412, October 2012. (28% acceptance rate)

C41. A. Pedram, A. Gerstlauer, R. A. van de Geijn, "On the Efficiency of Register File versus Broadcast Interconnect for Collective Communications in Data-Parallel Hardware Accelerators," *Proceedings of the IEEE/IFIP International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*, New York, NY, pp. 19-26, October 2012. (28% acceptance rate)

C40. A. Pedram, S. Z. Gilani, N. S. Kim, R. van de Geijn, M. Schulte, A. Gerstlauer, "A Linear Algebra Core Design for Efficient Level-3 BLAS," *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP)*, Delft, The Netherlands, pp. 149-152, July 2012. (poster presentation)

C39. K. He, A. Gerstlauer, M. Orshansky, "Low-Energy Signal Processing using Circuit-Level Timing-Error Acceptance," *Proceedings of the IEEE International Conference on Integrated Circuit Design and Technology (ICICDT)*, Austin, TX, 4 pages, May 2012. (invited paper)

C38. A. Gerstlauer, S. Chakravarty, M. Kathuria, P. Razaghi, "Abstract System-Level Models for Early Performance and Power Exploration," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Sydney, Australia, pp. 213-218, January 2012. (invited paper)

C37. P. Razaghi, A. Gerstlauer, "Automatic Timing Granularity Adjustment for Host-Compiled Software Simulation," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Sydney, Australia, pp. 567-572, January 2012. (34% acceptance rate)

C36. D. Pfeifer, A. Gerstlauer, "Expression-Level Parallelism for Distributed Spice Circuit Simulation," *Proceedings of the IEEE/ACM International Symposium on Distributed and Real Time Applications (DS-RT)*, Manchester, United Kingdom, pp. 12-17, September 2011.

C35. M. S. Lopez, A. Gerstlauer, A. Avila, S. O. Martinez-Chapa, "A Programmable and Configurable Multi-port System-on-Chip for Stimulating Electrokinetically-Driven Microfluidic Devices," *Proceedings of the International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, Boston, MA, pp. 8361-8364, September 2011.

C34. A. Abdel-Hadi, J. Michel, A. Gerstlauer, S. Vishwanath, "Real-Time Optimization of Video Transmission in a Network of AAVs," *IEEE Vehicular Technology Conference (VTC)*, San Francisco, CA, 5 pages, September 2011.

C33. A. Pedram, A. Gerstlauer, R. A. van de Geijn, "A High-Performance, Low-Power Linear Algebra Core," *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP)*, Santa Monica, CA, pp. 35-42, September 2011. (26% acceptance rate)

C32. J. Lin, A. Srivatsa, A. Gerstlauer, B. L. Evans "Heterogeneous Multiprocessor Mapping for Real-Time Streaming Systems," *Proceedings of the IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, Prague, Czech Republic, pp. 1605-1608, May 2011.

C31. P. Razaghi, A. Gerstlauer, "Host-Compiled Multicore RTOS Simulator for Embedded Real-Time Software Development," *Proceedings of the Design, Automation and Test in Europe (DATE) Conference*, Grenoble, France, 6 pages, March 2011. (27% acceptance rate)

C30. K. He, A. Gerstlauer, M. Orshansky, "Controlled Timing-Error Acceptance for Low Energy IDCT Design," *Proceedings of the Design, Automation and Test in Europe (DATE) Conference*, Grenoble, France, 6 pages, March 2011. (27% acceptance rate)

C29. R. Dömer, W. Chen, X. Han, A. Gerstlauer, "Multi-Core Parallel Simulation of System-Level Description Languages," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Yokohama, Japan, pp. 311-316, January 2011. (invited paper)

C28. J. Gladigau, A. Gerstlauer, C. Haubelt, M. Streubühr, J. Teich, "A System-Level Synthesis Approach from Formal Application Models to Generic Bus-Based MPSoCs," *Proceedings of the IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS)*, Samos, Greece, pp. 118-125, July 2010.

C27. A. Gerstlauer, "Host-Compiled Simulation of Multi-Core Platforms," *Proceedings of the IEEE/IFIP International Symposium on Rapid System Prototyping (RSP)*, Washington, DC, 6 pages, June 2010. (invited paper)

C26. A. Gerstlauer, G. Schirner, "Platform Modeling for Exploration and Synthesis," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Taipei, Taiwan, pp. 725-731, January 2010. (invited paper)

C25. G. Schirner, A. Gerstlauer, R. Dömer, "System-Level Development of Embedded Software," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Taipei, Taiwan, pp. 903-909, January 2010. (invited paper)

C24. A. Pedram, D. Craven, A. Gerstlauer, "Modeling Cache Effects at the Transaction Level," *Analysis, Architectures and Modeling of Embedded Systems*, Proceedings of the IFIP International Embedded Systems Symposium (IESS), Langenargen, Germany, edited by Achim Rettberg, Mauro Zanella, Michael Amann, Michael Keckeisen, Franz Rammig, vol. 310 of IFIP Advances in Information and Communication Technology, Springer, ISBN 978-3-642-04283-6, pp. 89-101, September 2009. (**best paper runner-up**)

C23. A. Banerjee, A. Gerstlauer, "Transaction Level Modeling of Best-Effort Channels for Networked Embedded Devices," *Analysis, Architectures and Modeling of Embedded Systems*, Proceedings of the IFIP International Embedded Systems Symposium (IESS), Langenargen, Germany, edited by Achim Rettberg, Mauro Zanella, Michael Amann, Michael Keckeisen, Franz Rammig, vol. 310 of IFIP Advances in Information and Communication Technology, Springer, ISBN 978-3-642-04283-6, pp. 77-88, September 2009.

C22. R. Dömer, A. Gerstlauer, W. Mueller, "Introduction to Hardware-Dependent Software Design," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Yokohama, Japan, pp. 290-292, January 2009. (invited paper)

C21. A. Gerstlauer, J. Peng, D. Shin, D. Gajski, A. Nakamura, D. Araki, Y. Nishihara, "Specify-Explore-Refine (SER): From Specification to Implementation," *Proceedings of the ACM/IEEE Design Automation Conference (DAC)*, Anaheim, CA, pp. 586-591, June 2008. (invited paper)

C20. G. Schirner, A. Gerstlauer, R. Dömer, "Automatic Generation of Hardware Dependent Software for MPSoCs from Abstract System Specifications," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Seoul, South Korea, pp. 271-276, January 2008. (29% acceptance rate)

C19. G. Schirner, G. Sachdeva, A. Gerstlauer, R. Dömer, "Embedded Software Development in a System-Level Design Flow," *Embedded System Design: Topics, Techniques and Trends*, Proceedings of the IFIP International Embedded Systems Symposium (IESS), Irvine, CA, edited by A. Rettberg, M. Zanella, R. Dömer, A. Gerstlauer, F. Rammig, vol. 231 of IFIP Advances in Information and Communication Technology, Springer, ISBN 978-0-387-72257-3, pp. 289-298, June 2007.

C18. D. Shin, A. Gerstlauer, R. Dömer, D. D. Gajski, "An Interactive Design Environment for C-based High-Level Synthesis," *Embedded System Design: Topics, Techniques and Trends*, Proceedings of the IFIP International Embedded Systems Symposium (IESS), Irvine, CA, edited by A. Rettberg, M. Zanella, R. Dömer, A. Gerstlauer, F. Rammig, vol. 231 of IFIP Advances in Information and Communication Technology, Springer, ISBN 978-0-387-72257-3, pp. 135-144, June 2007.

C17. G. Schirner, A. Gerstlauer, R. Dömer, "Abstract, Multifaceted Modeling of Embedded Processors for System Level Design," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Yokohama, Japan, pp. 384-389, January 2007. (32% acceptance rate)

C16. R. Dömer, A. Gerstlauer, D. Shin, "Cycle-accurate RTL Modeling with Multi-Cycled and Pipelined Components," *Proceedings of the IEEE International SoC Design Conference (ISOCC)*, Seoul, Korea, 4 pages, October 2006.

C15. D. Shin, A. Gerstlauer, J. Peng, R. Dömer, D. D. Gajski, "Automatic Generation of Transaction Level Models for Rapid Design Space Exploration," *Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Seoul, Korea, pp. 64-69, October 2006. (25% acceptance rate)

C14. D. Shin, A. Gerstlauer, R. Dömer, D. D. Gajski, "Automatic Generation of Communication Architectures," *From Specification to Embedded Systems Application*, Proceedings of the IFIP International Embedded Systems Symposium (IESS), Manaus, Brazil, edited by A. Rettberg, M. C. Zanella, F. Rammig, vol. 184 of IFIP On-Line Library in Computer Science, Springer, ISBN 0-387-27557-6, pp. 179-188, September 2005.

C13. D. Shin, A. Gerstlauer, R. Dömer, D. D. Gajski, "Automatic Network Generation for System-On-Chip Communication Design," *Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Jersey City, NJ, pp. 255-260, September 2005. (25% acceptance rate)

C12. A. Gerstlauer, D. Shin, R. Dömer, D. D. Gajski, "System-Level Communication Modeling for Network-On-Chip Synthesis," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Shanghai, China, pp. 45-48, January 2005. (27% acceptance rate)

C11. L. Cai, A. Gerstlauer, D. Gajski, "Multi-Metric and Multi-Entity Characterization of Applications for Early System Design Exploration," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Shanghai, China, pp. 944-947, January 2005. (Poster, 40% acceptance rate)

C10. L. Cai, A. Gerstlauer, D. Gajski, "Retargetable Profiling for Rapid, Early System-Level Design Space Exploration," *Proceedings of the ACM/IEEE Design Automation Conference (DAC)*, San Diego, CA, pp. 281-286, June 2004. (20% acceptance rate)

C9. H. Yu, A. Gerstlauer, D. Gajski, "RTOS Scheduling in Transaction Level Models," *Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign & System Synthesis (CODES+ISSS)*, Newport Beach, CA, pp. 31-36, October 2003. (21% acceptance rate)

C8. A. Gerstlauer, H. Yu, D. D. Gajski, "RTOS Modeling for System Level Design," *Proceedings of the Design, Automation and Test in Europe (DATE) Conference*, Munich, Germany, pp. 130-135, March 2003. (17% acceptance rate) **Reprinted as [P3] in *The Most Influential Papers of 10 Years DATE*.**

C7. W. Mueller, R. Dömer, A. Gerstlauer, "The Formal Execution Semantics of SpecC," *Proceedings of the International Symposium on System Synthesis (ISSS)*, Kyoto, Japan, pp. 150-155, October 2002. (33% acceptance rate)

C6. A. Gerstlauer, D. D. Gajski, "System-Level Abstraction Semantics," *Proceedings of the International Symposium on System Synthesis (ISSS)*, Kyoto, Japan, pp. 231-236, October 2002. (33% acceptance rate)

C5. S. B. Saoud, D. D. Gajski, A. Gerstlauer, "Seamless Approach for the Design of Control Systems for Power Electronics and Electric Drives," *Proceedings of the IEEE International Conference on Systems, Man and Cybernetics (SMC)*, Hammamet, Tunisia, 6 pages, October 2002.

C4. S. B. Saoud, D. D. Gajski, A. Gerstlauer, "Co-Design of Embedded Controllers for Power Electronics and Electric Systems," *Proceedings of the IEEE International Symposium on Intelligent Control (ISIC)*, Vancouver, Canada, pp. 379-383, October 2002.

C3. S. B. Saoud, D. D. Gajski, A. Gerstlauer, "Co-Design of Emulators for Power Electric Processes Using SpecC Methodology," *Proceedings of the 28th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Sevilla, Spain, pp. 2143-2148, November 2002.

C2. A. Gerstlauer, S. Zhao, D. Gajski, A. Horak, "SpecC System-Level Design Methodology Applied to the Design of a GSM Vocoder," *Proceedings of the Ninth Workshop on Synthesis and System Integration of Mixed Technologies (SASIMI)*, Kyoto, Japan, 8 pages, April 2000.

C1. M. Bühler, A. Gerstlauer, B. Stöhr, U. G. Baitinger, "Eine geeignete Schaltkreistechnologie für einen 3D-SOI-Prozess mit T-Gate Transistoren" (in German), *8. ITG Fachtagung Mikroelektronik für die Informationstechnik*, Hannover, Germany, March 1998.

C. Other Major Publications

D2. R. Dömer, A. Gerstlauer, D. Gajski, "SpecC Language Reference Manual, Version 2.0," SpecC Technology Open Consortium (STOC), 151 pages, December 2002.

D1. R. Dömer, A. Gerstlauer, D. Gajski, "SpecC Language Reference Manual, Version 1.0," SpecC Technology Open Consortium (STOC), 84 pages, March 2001.

D. Books, Editor of Books

B7. D. D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, *Embedded System Design: Modeling, Synthesis, Verificatio*n, Springer, ISBN 978-1-4419-0503-1, 349 pages, September 2009.

B6. A. Rettberg, M. Zanella, R. Dömer, A. Gerstlauer, F. Rammig (editors), *Embedded System Design: Topics, Techniques and Trends*, Springer, ISBN 978-0-387-72257-3, 444 pages, June 2007.

B5. A. Gerstlauer, R. Dömer, J. Peng, D. D. Gajski, *System Design: A Practical Guide with SpecC*, Chinese Edition, Translated by Jinian Bian and Hongxi Xue, Tsinghua University Press, China, ISBN 978-7-302-13289-9, 260 pages, January 2008.

B4. A. Gerstlauer, R. Dömer, J. Peng, D. D. Gajski, *System Design: A Practical Guide with SpecC*, Japanese Edition, Translated by Tsuneo Kinoshita, SpecC Technology Open Consortium, Japan, 252 pages, June 2001.

B3. A. Gerstlauer, R. Dömer, J. Peng, D. D. Gajski, *System Design: A Practical Guide with SpecC*, Kluwer Academic Publishers, ISBN 0-7923-7387-1, 255 pages, June 2001.

B2. D. D. Gajski, J. Zhu, R. Dömer, A. Gerstlauer, S. Zhao, Spec*C: Specification Language and Methodology*, Japanese Edition, Translated by Tsuneo Kinoshita, CQ Publishing, Japan, ISBN 4-7898-3353-4, 309 pages, December 2000.

B1. D. D. Gajski, J. Zhu, R. Dömer, A. Gerstlauer, S. Zhao, *SpecC: Specification Language and Methodology*, Kluwer Academic Publishers, ISBN 0-7923-7822-9, 313 pages, March 2000.

E. Chapters of Books

P5. G. Schirner, R. Dömer, A. Gerstlauer, "High-Level Development, Modeling and Automatic Generation of Hardware-Dependent Software," in W. Ecker, W. Mueller, R. Dömer (eds.),

Hardware-Dependent Software: Principles and Practice, Springer, ISBN 978-1-4020-9435-4, pp. 203-231, January 2009.

P4. H. Zabel, W. Mueller, A. Gerstlauer, "Accurate RTOS Modeling and Analysis with SystemC," in W. Ecker, W. Mueller, R. Dömer (eds.), *Hardware-Dependent Software: Principles and Practice*, Springer, ISBN 978-1-4020-9435-4, pp. 233-260, January 2009.

P3. A. Gerstlauer, H. Yu, D. D. Gajski, "RTOS Modeling for System-Level Design," in R. Lauwereins, J. Madsen (eds.), *Design, Automation, and Test in Europe: The Most Influential Papers of 10 Years DATE*, Springer, ISBN 978-1-4020-6487-6, pp. 47-58, March 2008.

P2. A. Gerstlauer, H. Yu, D. D. Gajski, "RTOS Modeling for System-Level Design," in A. A. Jerraya, S. Yoo, N. When, D. Verkest (eds.), *Embedded Software for SoC*, Kluwer Academic Publishers, ISBN 1-4020-7528-6, pp. 55-68, June 2003.

P1. A. Rettberg, F. J. Rammig, A. Gerstlauer, D. D. Gajski, W. Hardt, B. Kleinjohann, "The Specification Language SpecC within the PARADISE Design Environment," in B. Kleinjohann (ed.), *Architecture and Design of Distributed Embedded Systems*, Kluwer Academic Publishers, ISBN 0-7923-7345-6, pp. 111-120, April 2001.

F. Workshop Proceedings

W4. J. Miao, A. Gerstlauer, M. Orshansky, "Modeling and Synthesis of Quality-Energy Optimal Approximate Adders," Work-in-Progress (WIP) session, *ACM/EDAC/IEEE Design Automation Conference (DAC)*, San Francisco, CA, June 2012.

W3. A. Pedram, A. Gerstlauer, R. van de Geijn, "Overcoming Register File Inefficiencies by Using 2D Broadcast Bus Interconnects in Linear Algebra Accelerators," *3rd Workshop on SoCs, Heterogenenous Architectures and Workloads (SHAW-3)*, New Orleans, LA, February 2012.

W2. R. Dömer, A. Gerstlauer, D. Gajski, "SpecC Methodology for High-Level Modeling," *9th IEEE/DATC Electronic Design Processes Workshop*, Monterey, CA, April 2002.

W1. R. Dömer, A. Gerstlauer, P. Kritzinger, M. Olivarez, "The SpecC System-Level Design Language and Methodology, Part 2", *Embedded Systems Conference (ESC)*, San Francisco, CA, March 2002

G. Technical Reports

R40. W.-C. Su, P. Razaghi, A. Sinha, A. Gerstlauer, "Design of Flexible Audio Processing Platforms using the System-on-Chip Environment," CERC, UT Austin, Technical Report UT-CERC-12-06, August 2012.

R39. M. Kathuria, A. Gerstlauer, "A Framework for Automation of System-Level Design Space Exploration," CERC, UT Austin, Technical Report UT-CERC-12-05, June 2012.

R38. A. Pedram, A. Gerstlauer, R. van de Geijn, "Co-Design Tradeoffs for High-Performance, Low-Power Linear Algebra Architectures," CERC, UT Austin, Technical Report UT-CERC-12-02, October 2011.

R37. A. Goswami, A. Gerstlauer, "ExtractCFG: A Framework to Enable Accurate Timing Back Annotation of C Language Source Code," CERC, UT Austin, Technical Report UT-CERC-11-02, August 2011.

R36. H. Park, X. Shen, H. Vikalo, A. Gerstlauer, "Algorithm/Architecture Co-Design of a Stochastic Simulation System-on-Chip," CERC, UT Austin, Technical Report UT-CERC-11-01, January 2011.

R35. A. Pedram, A. Gerstlauer, R. van de Geijn, "Towards a High-Performance, Low-Power Linear Algebra Processor," CERC, UT Austin, Technical Report UT-CERC-10-03, September 2010.

R34. P. S. Bomfim, A. Gerstlauer, "Integration of Virtual Platform Models into a System-Level Design Framework," CERC, UT Austin, Technical Report UT-CERC-10-02, August 2010.

R33. A. Gerstlauer, D. Shin, S. Abdi, P. Chandraiah, D. Gajski, "Design of a MP3 Decoder using the System-On-Chip Environment (SCE)," Technical Report CECS-TR-07-05, Center for Embedded Computer Systems, UC Irvine, October 2007.

R32. A. Gerstlauer, G. Schirner, D. Shin, J. Peng, R. Dömer, D. Gajski, "System-On-Chip Component Models," Technical Report CECS-TR-06-10, Center for Embedded Computer Systems, UC Irvine, May 2006.

R31. E.J. Johnson, A. Gerstlauer, R. Doemer, "Efficient Debugging and Tracing of System Level Designs," Technical Report CECS-TR-06-08, Center for Embedded Computer Systems, UC Irvine, May 2006.

R30. G. Schirner, G. Sachdeva, A. Gerstlauer, R. Dömer, "Modeling, Simulation and Synthesis in an Embedded Software Design Flow for an ARM Processor," Technical Report CECS-TR-06-06, Center for Embedded Computer Systems, UC Irvine, May 2006.

R29. A. Gerstlauer, G. Schirner, D. Shin, J. Peng, "Necessary and Sufficient Functionality and Parameters for SoC Communication," Technical Report CECS-TR-06-01, Center for Embedded Computer Systems, UC Irvine, May 2006.

R28. D. Gajski, A. Gerstlauer, R. Dömer, S. Abdi, J. Peng, D. Shin, "TL Environment," Technical Report CECS-TR-05-10, Center for Embedded Computer Systems, UC Irvine, July 2005.

R27. D. Shin, A. Gerstlauer, R. Dömer, D. Gajski, "System-on-Chip Communication Modeling Style Guide," Technical Report CECS-TR-04-25, Center for Embedded Computer Systems, UC Irvine, July 2004.

R26. D. Shin, L. Cai, A. Gerstlauer, R. Dömer, D. Gajski, "System-on-Chip Transaction-Level Modeling Style Guide," Technical Report CECS-TR-04-24, Center for Embedded Computer Systems, UC Irvine, July 2004.

R25. D. Shin, J. Peng, A. Gerstlauer, R. Dömer, D. Gajski, "System-on-Chip Network Modeling Style Guide," Technical Report CECS-TR-04-23, Center for Embedded Computer Systems, UC Irvine, July 2004.

R24. J. Peng, A. Gerstlauer, R. Dömer, D. Gajski, "System-on-Chip Architecture Modeling Style Guide," Technical Report CECS-TR-04-22, Center for Embedded Computer Systems, UC Irvine, July 2004.

R23. R. Dömer, A. Gerstlauer, D. Shin, "Cycle-accurate RTL Modeling with Multi-Cycled and Pipelined Components," Technical Report CECS-TR-04-19, Center for Embedded Computer Systems, UC Irvine, July 2004.

R22. D. Shin, A. Gerstlauer, D. Gajski, "Communication Link Synthesis for SoC," Technical Report CECS-TR-04-16, Center for Embedded Computer Systems, UC Irvine, June 2004.

R21. D. Shin, A. Gerstlauer, D. Gajski, "Network Synthesis for SoC," Technical Report CECS-TR-04-15, Center for Embedded Computer Systems, UC Irvine, June 2004.

R20. L. Cai, A. Gerstlauer, D. Gajski, "Retargetable Profiling for Rapid, Early System-Level Design Space Exploration," Technical Report CECS-TR-04-04, Center for Embedded Computer Systems, UC Irvine, October 2003.

R19. D. Shin, A. Gerstlauer, R. Dömer, D. Gajski, "C-Based Interactive RTL Design Methodology," Technical Report CECS-TR-03-42, Center for Embedded Computer Systems, UC Irvine, December 2003.

R18. A. Gerstlauer, "Communication Abstractions for System-Level Design and Synthesis," Technical Report CECS-TR-03-30, Center for Embedded Computer Systems, UC Irvine, October 2003.

R17. A. Gerstlauer, L. Cai, D. Shin, R. Dömer, D. Gajski, "System-On-Chip Component Models," Technical Report CECS-TR-03-26, Center for Embedded Computer Systems, UC Irvine, August 2003.

R16. S. Abdi, J. Peng, H. Yu, D. Shin, A. Gerstlauer, R. Dömer, D. Gajski, "System-On-Chip Environment (SCE Version 2.2.0 Beta): Tutorial," Technical Report CECS-TR-03-41, Center for Embedded Computer Systems, UC Irvine, July 2003.

R15. A. Gerstlauer, K. Ramineni, R. Dömer, D. Gajski, "System-On-Chip Specification Style Guide," Technical Report CECS-TR-03-21, Center for Embedded Computer Systems, UC Irvine, June 2003.

R14. H. Yu, A. Gerstlauer, D. Gajski, "RTOS Scheduling in Transaction Level Models," Technical Report CECS-TR-03-12, Center for Embedded Computer Systems, UC Irvine, March 2003.

R13. D. Gajski, J. Peng, A. Gerstlauer, H. Yu, D. Shin, "System Design Methodology and Tools," Technical Report CECS-TR-03-02, Center for Embedded Computer Systems, UC Irvine, January 2003.

R12. S. Abdi, J. Peng, R. Dömer, D. Shin, A. Gerstlauer, A. Gluhak, L.Cai, Q. Xie, H. Yu, P. Zhang, D. Gajski, "System-On-Chip Environment (SCE): Tutorial," Technical Report CECS-TR-02-28, Center for Embedded Computer Systems, UC Irvine, September 2002.

R11. A. Gerstlauer, D. Gajski, "System-Level Abstraction Semantics," Technical Report CECS-TR-02-17, Center for Embedded Computer Systems, UC Irvine, July 2002.

R10. A. Gerstlauer, "SpecC Modeling Guidelines," Technical Report CECS-TR-02-16, Center for Embedded Computer Systems, UC Irvine, April 2002.

R9. J. Peng, L. Cai, A. Gerstlauer, D. Gajski, "Interactive System Design Flow," Technical Report CECS-TR-02-15, Center for Embedded Computer Systems, UC Irvine, April 2002.

R8. W. Mueller, R. Dömer, D. Gajski, "The Formal Execution Semantics of SpecC," Technical Report CECS-TR-02-04, Center for Embedded Computer Systems, UC Irvine, January 2002.

R7. W. Mueller, R. Dömer, A. Gerstlauer, "The Formal Execution Semantics of SpecC," Technical Report ICS-TR-01-59, Information and Computer Science, UC Irvine, November 2001.

R6. A. Gerstlauer, "SpecC Modeling Guidelines," Technical Report ICS-TR-00-48, Center for Embedded Computer Systems, UC Irvine, August 2000.

R5. A. Gerstlauer, "Communication Software Code Generation," Technical Report ICS-TR-00-46, Information and Computer Science, UC Irvine, August 2000.

R4. D. Gajski, J. Zhu, R. Dömer, A. Gerstlauer, S. Zhao, "The SpecC Methodology," Technical Report ICS-TR-99-56, Information and Computer Science, UC Irvine, December 1999.

R3. L. Cai, J. Peng, C. Chang, A. Gerstlauer, H. Li, A. Selka, C. Siska, L. Sun, S. Zhao, D. Gajski, "Design of a JPEG Encoding System," Technical Report ICS-TR-99-54, Information and Computer Science, UC Irvine, November 1999.

R2. A. Gerstlauer, S. Zhao, D. Gajski, A. M. Horak, "Design of a GSM Vocoder using SpecC Methodology," Technical Report ICS-TR-99-11, Information and Computer Science, UC Irvine, March 1999.

R1. A. Gerstlauer, S. Zhao, D. Gajski, "VHDL+/SpecC Comparisons - A Case Study," Technical Report ICS-TR-98-23, Information and Computer Science, UC Irvine, May 1998.

ORAL PRESENTATIONS:

A. Tutorials

8. "Designing Multi-Processor and Multi-Core Systems-on-Chip," embedded tutorial, Austin Conference on Integrated Systems and Circuits (ACISC), Austin, Texas, October 2009.
7. "Modeling, Synthesis and Verification," in System-Level Modeling, Analysis and Synthesis of Embedded Multi-core Designs, full-day tutorial with S. Abdi, C. Haubelt, W. Ecker, M. Meredith, M. Speitel, J. Teich, D. Gajski (organizer), Design, Automation and Test in Europe (DATE) Conference, Nice, France, April 2009.
6. "Principles of Embedded Systems: Modeling, Synthesis and Verification," in High-Level Design, two-day tutorial with M. Fujita (organizer), D. Gajski, S. Abdi, VLSI Design Education Center (VDEC), Tokyo, Japan, January 2008.

5. "Embedded System Modeling," in Concepts and Tools for Practical Embedded System Design, half-day tutorial with S. Abdi, D. Gajski, N. Dutt (organizer), IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC), Yokohama, Japan, January 2007.
4. "System-Level Modeling and Design: Experimentation with SpecC," in System Level Specification beyond RTL, half-day tutorial with J. Zhu, A. Jerraya, D. Gajski (organizer), Design, Automation and Test in Europe (DATE) Conference, Paris, France, March 2002.
3. "Modeling and Design with SpecC" and "Design of a GSM Vocoder," in SpecC Language and Design Methodology, half-day tutorial with T. Ishii, J. Zhu, D. Gajski (organizer), Design, Automation and Test in Europe (DATE) Conference, Munich, Germany, March 2001.
2. "Modeling and Design with SpecC" and "Design of a GSM Vocoder," in SpecC Language and Design Methodology, two-day tutorial with R. Dömer, D. Gajski, Motorola Semiconductor Products Section, Austin, April 2001.
1. "Modeling and Design with SpecC," in SpecC Language and Design Methodology, full-day tutorial with T. Ishii, J. Zhu, M. Olivarez, C. Siska, D. Araki, D. Gajski (organizer), IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC), Yokohama, Japan, January 2001.

B. Workshop Presentations

3. "Dataparallel Accelerator Design beyond GPUs," IEEE Central Texas Section CAS/SSC/CEDA Workshop on Data Parallelism for Multi-Core Chips and GPU, Austin, TX, October 2012.
2. "Teaching Experience: Developing a Class on Embedded Systems," in *Young Faculty Workshop*, ACM/EDAC/IEEE Design Automation Conference (DAC), San Francisco, June 2012.
1. "OS and Processor Modeling," in workshop on *Hardware Dependent Software (HdS)*, ACM/IEEE Design Automation Conference (DAC), San Diego, June 2007.

C. Keynotes and Distinguished Lectures

1. "Software Synthesis for Embedded Multicore Systems," Keynote, Brazilian Symposium on Computing System Engineering (SBESC), Florianopolis, Brazil, November 2011.

D. Invited Talks

48. "System-Level Design of Embedded Systems," Department of Electrical Engineering and Information Technology, Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany, June 2013.
47. "Models and Architectures for Heterogeneous System Design," Department of Computer Science, University of California, Los Angeles, Los Angeles, CA, May 2013.
46. "Host-Compiled System Models for Early Power and Performance Exploration," Qualcomm Technologies (QCT), Inc., San Diego, CA, May 2013.
45. "Models and Architectures for Heterogeneous System Design," Department of Computer Science and Engineering, University of California, San Diego, San Diego, CA, May 2013.
44. "Models and Architectures for Heterogeneous System Design," Center for Embedded Computer Systems (CECS), University of California, Irvine, Irvine, CA, May 2013.
43. "Models and Architectures for Heterogeneous System Design," Center for Experimental Research in Computer Systems (CERCS), Georgia Institute of Technology, Atlanta, GA, April 2013.
42. "Models and Architectures for Heterogeneous System Design," Design of Robotics and Embedded Systems, Analysis and Modeling Seminar (DREAMS), Center for Electronic System Design/Center for Hybrid and Embedded Software Systems (CHESS), University of California, Berkeley, Berkeley, CA, April 2013.
41. "Models and Architectures for Heterogeneous System Design," Center for Silicon System Implementation (CSSI), Carnegie Mellon University, Pittsburgh, PA, April 2013.
40. "Heterogeneous System Design," Intel Research, Hillsboro, Oregon, March 2012.

39. "A Low-Power, High-Performance Linear Algebra Core," NSF Center for Embedded Systems, Faculty of Computer Science and Engineering, Arizona State University, February 2012.
38. "A Low-Power, High-Performance Linear Algebra Core," Tech Topics Seminar Series, Advanced Micro Devices (AMD), Austin, TX, November 2011.
37. "Circuit-Level Timing-Error Acceptance for Low Energy Signal Processing," Cirrus Logic, Austin, TX, November 2011.
36. "Using Cutting-Edge Tools for Communication System Design," National Instruments NIWeek conference, Austin, TX, August 2011.
35. "System-Level Design of Heterogeneous Embedded Multi-Core Platforms," Department of Informatics, University of Tübingen, Germany, June 2011.
34. "Low Power, High Performance Linear Algebra Processing," IBM Austin Research Lab, Austin, Texas, May 2011.
33. "System-Level Design of Heterogeneous Embedded Multi-Core Platforms," Huawei Technologies USA, Dallas, Texas, March 2011.
32. "Embedded System Design Challenges and Trends," Texas Instruments, Dallas, Texas, March 2011.
31. "Embedded Systems Research," 3M, Austin, Texas, January 2011.
30. "System-Level Design of Multi-Processor/Multi-Core Systems-on-Chip," Intel Research, Hillsboro, Oregon, November 2010.
29. "System-Level Design for Heterogeneous Low-Power and High-Performance Compute Fabrics," National Instruments, Austin, Texas, October 2010.
28. "Heterogeneous Computing and the System-Level Design Challenge," Advanced Micro Devices (AMD), Austin, Texas, August 2010.
27. "System-Level Design of Embedded Multi-Processor/Multi-Core Systems-on-Chip," National Instruments, Berkeley Research Lab, June 2010.
26. "System-Level Design of Multi-Processor/Multi-Core System-on-Chip," Qualcomm, Bay Area Research and Development group, June 2010.
25. "Designing Multi-Processor and Multi-Core Systems-on-Chip," IEEE Central Texas SSC/CAS Chapter, Austin, Texas, February, 2010.
24. "Electronic System Level Modeling for Automated MPSoC Design and Exploration," IBM Research & Development, Böblingen, Germany, August 2009.
23. "High-Level Programming, Prototyping and Synthesis of MPSoC Software," Department of Computer Science, University of Erlangen-Nuremberg, Germany, July 2009.
22. "Electronic System Level Modeling for Automated MPSoC Design and Exploration," Freescale, Austin, TX, January 2009.
21. "High-Level Programming, Prototyping and Synthesis of MPSoC Software," Department of Embedded/Real-Time Systems, University of Ulm, Germany, December 2008.
20. "Electronic System Level Modeling for Automated, C-Based MPSoC Design and Exploration," IBM Austin Research Labs, December 2008.
19. "Electronic System Level Modeling, Design and Synthesis of Embedded Computer Systems," National Instruments, Austin, TX, November 2008.
18. "System-Level Modeling for Embedded System Design Automation," Department of Electrical and Computer Engineering, Florida International University, April 2008.
17. "System-Level Modeling for Embedded System Design Automation," Department of Electrical Engineering, University of Hawaii at Manoa, April 2008.
16. "System-Level Modeling for Embedded System Design Automation," Department of Electrical and Computer Engineering, University of Texas at Austin, March 2008.
15. "System-Level Modeling for Embedded System Design Automation," Department of Computer Science and Engineering, University of Texas at Arlington, March 2008.

14. "Automated, C-Based Design of Multi-Processor Systems-On-Chip", Department of Computer Science, University of Erlangen-Nuremberg, Germany, March 2008.
13. "System-Level Modeling for Embedded System Design Automation," Department of Electrical Engineering and Computer Science, University of Kansas, Lawrence, February 2008.
12. "Programming, Modeling and Synthesis of Multi-Processor System Software," Electronics Design Seminar, Department of Electrical and Computer Engineering, University of California, Santa Barbara, February 2008.
11. "Embedded Processor and RTOS Modeling for Rapid, Early MPSoC Design and Validation," Fujita lab, University of Tokyo, Japan, August 2007.
10. "Embedded Processor and RTOS Modeling for Multi-Processor Design and Validation," Institute of Computer Architecture and Computer Engineering, University of Stuttgart, Germany, June 2007.
9. "Embedded Processor and RTOS Modeling for Multi-Processor Design and Validation," Department for Base Technologies & Services, Infineon Technologies AG, Munich, Germany, June 2007.
8. "Embedded Processor and RTOS Modeling for Rapid, Early MPSoC Design and Validation," Institute for Integrated Systems, Munich University of Technology, Munich, Germany, June 2007.
7. "Modeling of Embedded Processors and Real-Time Operating Systems for Rapid, Early Multi-Processor Systems Design and Validation," C-LAB, University of Paderborn, Germany, June 2007.
6. "A System Design Environment for Automatic Model Generation and Prototyping," Research and Advance Development, Robert Bosch GmbH, Schwieberdingen, Germany, March 2006.
5. "Layer-Based Communication Design for Automatic SoC Platform Generation," Department of Computer Engineering, University of Tübingen, October 2005.
4. "Methodology and Environment for System-Level Design," Xilinx Research Laboratories, San Jose, CA, August 2003.
3. "System-Level Design Language, Methodology and Environment," IBM Research and Development, Böblingen, Germany, March 2003.
2. "System-Level Design Language, Methodology and Environment," BMW, Munich, Germany, January 2003.
1. "Modeling and Design with SpecC," C-LAB, University of Paderborn, Germany, March 2001.

PATENTS:

None

IN-RANK GRANTS AND CONTRACTS:

Co-Investigators	Title	Agency	Grant Total	Grant Period
-	Core Technology Development for System Simulation including Network	Samsung Electronics Co., Ltd., DMC R&D Center, Korea	$149,020	6/1/2013-12/31/2013
-	Automated Design Space Exploration and Optimization of DSP Systems	National Instruments, Inc.	$60,000	8/1/2012-7/31/2013
Heath, Robert (PI)	Interference Alignment in Distributed Environments	Army Research Office (ARO)	$99,980 ($49,990)	9/1/2012-8/31/2013

John, Lizy	Multi-dimensional Modeling, Design and Exploration of Heterogeneous Multicore SoCs	Semiconductor Research Corporation (SRC)	$345,000 ($173,000)	8/1/2012–7/31/2015
Heath, Robert (PI)	Interference Alignment in Distributed Environments	Defense Advanced Research Projects Agency (DARPA)	$99,344 ($49,672)	9/1/2011-8/31/2012
-	Towards Enabling Full-Cell Biochemical Network Simulations	UT Austin, Summer Research Assignment	$20,000	7/1/2011-8/31/2011
van de Geijn, Robert	SHF: Small: Algorithm/Architecture Co-Design of Low Power and High Performance Linear Algebra Compute Fabrics	National Science Foundation (NSF)	$499,919 ($249,959)	6/1/2012-5/31/2015
Orshansky, Michael	SHF: Small: Formal Synthesis of Low-Energy Signal Processing Systems Relying on Controlled Timing-Error Acceptance	National Science Foundation (NSF)	$449,614 ($224,807)	9/1/2010-8/31/2013
-	Automatic Platform Model Calibration and Tuning	Semiconductor Research Corporation (SRC)	$254,337	8/1/2010-7/31/2013

IN-RANK GIFTS:

Co-Investigators	Title	Company	Gift Total	Gift Period
Pingali, Keshav	Adaptive Hardware/Software Platforms for Mobile Web Browsing	Qualcomm, Inc., Bay Area Research Division (BARD)	$80,000 ($40,000)	1/1/2012-12/31/2012
-	Automated Design Space Exploration and Optimization of DSP Systems	National Instruments, Inc.	$40,000	8/1/2011-7/31/2012
-	Compiler-Assisted MPSoC Assembly and Mapping	Intel Labs	$46,000	1/1/2011-12/31/2012
-	Equipment Grant	Intel	$28,678	7/14/2009
IN-RANK FUNDING (my share):			**$2,171,892 ($1,385,463)**	

PREVIOUS GRANTS AND CONTRACTS:

Co-Investigators	Title	Agency	Grant Total	Grant Period
Daniel D. Gajski (PI)	SER Upgrades and Extensions	InterDesign Technologies, Inc. / Japanese Aerospace Exploration Agency (JAXA)	$1,390,000 ($695,000)	6/1/2006-5/31/2008
TOTAL FUNDING (my share):			**$3,561,892 ($2,080,463)**	

IN-KIND DONATIONS:

Co-Investigators	Equipment	Company	Value	Date
-	Prototyping boards and software licenses for SoC teaching lab	Xilinx, Inc.	$9,781	9/2010, 3/2013
-	Various test equipment (logic analyzers, function generators, oscilloscopes) for Digital Integrated Circuits and Systems lab	Dell, Inc.	$300,659	5/2011

PH.D. SUPERVISIONS COMPLETED:

Pedram, Ardavan	Algorithm/Architecture Codesign of Low Power and High Performance Linear Algebra Compute Fabrics (co-supervisor w/ Prof. van de Geijn, Computer Science)	Electrical and Computer Engineering	Univ. of Texas at Austin	2013
He, Ku	Adaptive Low-Energy Techniques in Memory and Digital Signal Processing Design (co-supervisor w/ Prof. Orshansky)	Electrical and Computer Engineering	Univ. of Texas at Austin	2012
Abdel Hadi, Ahmed	Multicast Networks: Capacity, Algorithms and Implementation (co-supervisor w/ Prof. Vishwanath)	Electrical and Computer Engineering	Univ. of Texas at Austin	2011
Salome Lopez De La Fuente, Martha	Definition, Design and Implementation of a Processor-Based Stimulation System for Electrokinetically-Driven Fluidic Devices (co-supervised w/ Prof. O. Martinez Chapa)	Information Technologies & Communications	Monterey Inst. of Technology, Mexico	2011
Schirner, Gunar	Improving Accuracy of Transaction Level Models in System-on-Chip Design (co-supervisor w/ Prof. Dömer)	Electrical Engineering and Computer Science	University of California, Irvine	2008

M.S. SUPERVISIONS COMPLETED:

Miao, Jin	Modeling and Synthesis of Quality-Energy Optimal Approximate Adders (co-supervisor w/ Prof. Orshansky)	Electrical and Computer Engineering	Univ. of Texas at Austin	2012
Sinha, Ashmita	Multi-Objective Trade-Off Exploration For Cyclo-Static And Synchronous Dataflow Graphs	Electrical and Computer Engineering	Univ. of Texas at Austin	2012
Kathuria, Manan	Framework for Automation of System-level Design Space Exploration	Electrical and Computer Engineering	Univ. of Texas at Austin	2012
Goswami, Arindam	ExtractCFG: A Framework to Enable Accurate Timing Back Annotation of C Language Source Code	Electrical and Computer Engineering	Univ. of Texas at Austin	2011
Tourish, John Patrick	dspIP: A TCP/IP Implementation for a Digital Signal Processor,	Electrical and Computer Engineering	Univ. of Texas at Austin	2011

Bomfim, Pablo Salinas	Integration of Virtual Platform Models into a System-Level Design Framework	Electrical and Computer Engineering	Univ. of Texas at Austin	2010
Williams, Joel	Prototyping of MP3 Decoding and Playback on an ARM-based FPGA Development Board	Electrical and Computer Engineering	Univ. of Texas at Austin	2010
Overholt, Peter James	Desktop Simulation of a Digital Signal Processing Design Flow using Synchronous Dataflow Modeling	Electrical and Computer Engineering	Univ. of Texas at Austin	2009

PH.D. IN PROGRESS:

A. Students admitted to candidacy

Miao, Jin (co-supervised w/ Prof. Orshansky)
Pfeifer, Dylan (part-time, co-supervised w/ Prof. Valvano)
Razaghi, Parisa

B. Post M.S. students preparing to take Ph.D. qualifying exam

Chakravarty, Suhas (part-time)
Lee, Dongwook
Lee, Seogoo
Park, Hyungman

M.S. IN PROGRESS:

Yu, Wenxiao
Zhao, Zhuoran

VITA:

Andreas Gerstlauer is an Assistant Professor in Electrical and Computer Engineering at The University of Texas at Austin. He received his Dipl.-Ing. degree in Electrical Engineering from the University of Stuttgart, Germany in 1997 and M.S. and Ph.D. degrees in Information and Computer Science from the University of California, Irvine (UCI) in 1998 and 2004, respectively. Prior to joining UT Austin in 2008, he was an Assistant Researcher in the Center for Embedded Computer Systems (CECS) at UC Irvine, leading a research group to develop electronic system-level (ESL) design tools. Commercial derivatives of such tools are in use at the Japanese Aerospace Exploration Agency (JAXA) and NEC Toshiba Space Systems among others.

Dr. Gerstlauer is co-author on 3 books and more than 60 conference and journal publications, and his paper on OS modeling was reprinted as one of the most influential contributions at DATE. He has presented in numerous conference and industrial tutorials, and serves on the program committee of major conferences such as DAC, DATE and CODES+ISSS. Dr. Gerstlauer's research interests include system-level design automation, system modeling, design languages and methodologies, and embedded hardware and software synthesis.

ANDREAS GERSTLAUER
Co-Authored Works

In the following, co-authors and relative contributions for collaborative journal and conference papers published while in rank are identified. The list only includes papers authored with collaborators other than my own students. Paper indices refer back to the full publication record in my CV.

COLLABORATORS (in rank):

A. Current or Former Students (at UT Austin)

A. Abdel-Hadi (co-supervised w/ S. Vishwanath), now a Post-doc at Virginia Tech
S. Chakravarty, now part-time at Freescale, India
K. He (co-supervised w/ M. Orshansky), now at Cirrus Logic, Austin, TX
M. Kathuria, now at Intel Mobile Communications, NJ.
D. Lee
S. Lee
M. S. Lopez (co-advisor w/ S. O. Martinez-Chapa, Monterrey Tech, Mexico), now at the Universidad de Monterrey, Mexico
J. Miao (co-supervised w/ M. Orshansky)
H. Park
A. Pedram (co-supervised w/ Prof. van de Geijn)
D. Pfeifer (part-time, co-supervised w/ Prof. Valvano)
P. Razaghi
Z. Zhao

B. Faculty Colleagues (at UT Austin)

D. Chiou, Electrical and Computer Engineering (ECE)
B. L. Evans, Electrical and Computer Engineering (ECE)
R. van de Geijn, Computer Science (CS)
R. W. Heath, Electrical and Computer Engineering (ECE)
M. Orshansky, Electrical and Computer Engineering (ECE)
J. Valvano, Electrical and Computer Engineering (ECE)
S. Vishwanath, Electrical and Computer Engineering (ECE)

C. Advisors

D. D. Gajski, Professor, UC Irvine

D. Other Students

A. Banerjee, M.S. Student, UT Austin, now India
W. Chen, Ph.D. Student, UC Irvine
D. Craven, M.S. Student, UT Austin
S. Z. Gilani, Ph.D. Student, University of Wisconsin-Madison
J. Gladigau, Ph.D. Student, University of Erlangen-Nuremberg, Germany
X. Han, Ph.D. Student, UC Irvine
J. Lin, Ph.D. Student, UT Austin (supervised by B. L. Evans)
A. Mariano, Universidade do Minho, Portgual (visiting M.S. student at UT Austin), now at TU Darmstadt, Germany
J. Michel, Ph.D. Student, UT Austin (supervised by C. Julien)
J. W. Massey, Ph.D. Student, UT Austin (supervised by R. W. Heath)
A. Srivatsa, M.S. Student, UT Austin, now at Rice University
J. Starr, M.S. Student, UT Austin (supervised by R. W. Heath), now at Kuma Signals, Austin, TX
M. Streubühr, Ph.D. Student, University of Erlangen-Nuremberg, Germany

E. Other Collaborators

A. Avila, Professor, Monterrey Tech, Mexico
J. McCalpin, Texas Advanced Computing Center (TACC), UT Austin
R. Dömer, Associate Professor, UC Irvine (former colleague)
N. S. Kim, Assistant Professor, University of Wisconsin-Madison
G. Schirner, Assistant Professor, Northeastern University (former student)
C. Haubelt, Professor, University of Rostock, Germany
S. O. Martinez-Chapa, Professor, Monterrey Tech, Mexico
W. Mueller, Researcher, C-LAB, Paderborn University, Germany
A. D. Pimentel, Associate Professor, University of Amsterdam, Netherlands
M. Schulte, Advanced Micro Devices (AMD) Research, Austin, TX
T. Stefanov, Leiden University, Netherlands
J. Teich, Professor, University of Erlangen-Nuremberg, Germany

CO-AUTHORED PUBLICATIONS (in rank):

A. Refereed Archival Journal Publications

J12. D. Pfeifer, J. Valvano, A. Gerstlauer, **[60%/20%/20%]** "SimConnect and SimTalk for Distributed Cyber-Physical System Simulation," *Simulation: Transactions of the Society for Modeling and Simulation International*, accepted for publication, November 2012.

J11. K. He, A. Gerstlauer, M. Orshansky, **[40%/30%/30%]** "Circuit-Level Timing-Error Acceptance for Design of Energy-Efficient DCT/IDCT-based Systems," *IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)*, vol. 23, no. 6, pp. 961-974, June 2013

J10. J. Lin, A. Gerstlauer, B. L. Evans, **[60%/30%/10%]** "Communication-Aware Heterogeneous Multiprocessor Mapping for Real-Time Streaming Systems," *Journal of Signal Processing Systems*, vol. 69, no. 3, pp. 279-291, December 2012.

J9. A. Pedram, R. A. van de Geijn, A. Gerstlauer, **[40%/30%/30%]** "Codesign Tradeoffs for High-Performance, Low-Power Linear Algebra Architectures," *IEEE Transactions on Computers (TC)*, special issue on Energy Efficient Computing, vol. 61, no. 12, pp. 1724-1736, December 2012.

J8. P. Razaghi, A. Gerstlauer, **[70%/30%]** "Predictive OS Modeling for Host-Compiled Simulation of Periodic Real-Time Task Sets," *IEEE Embedded System Letters*, vol. 4, no. 1, pp. 5-8, March 2012.

J7. J. Gladigau, A. Gerstlauer, C. Haubelt, M. Streubühr, J. Teich, **[30%/20%/20%/30%/0%]** "Automatic System-Level Synthesis: From Formal Application Models to Generic Bus-Based MPSoCs," *Transactions on High-Performance Embedded Architectures and Compilers (Transactions on HiPEAC)*, vol. 5, no. 4, 22 pages, 2011.

J6. G. Schirner, A. Gerstlauer, R. Dömer, **[40%/30%/30%]** "Fast and Accurate Processor Models for Efficient MPSoC Design," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 15, no. 2, article no. 10, pp. 1-26, February 2010.

J5. A. Gerstlauer, C. Haubelt, A. D. Pimentel, T. P. Stefanov, D. D. Gajski, J. Teich, **[30%/30%/30%/10%/0%/0%]** "Electronic System-Level Synthesis Methodologies," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 28, no. 10, pp. 1517-1530, October 2009.

J4. R. Dömer, A. Gerstlauer, J. Peng, D. Shin, L. Cai, H. Yu, S. Abdi, D. D. Gajski, **[20%/20%/10%/10%/10%/10%/10%/10%]** "System-on-Chip Environment: A SpecC-based Framework for Heterogeneous MPSoC Design," *EURASIP Journal on Embedded Systems (JES)*, vol. 2008, Article ID 647953, 13 pages, 2008.

B. Refereed Conference Proceedings

C54. J. Miao, A. Gerstlauer, M. Orshansky, **[50%/20%/30%]** "Approximate Logic Synthesis under General Error Magnitude and Frequency Constraints," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, November 2013.

C53. S. Lee, A. Gerstlauer, **[70%/30%]** "Fine Grain Word Length Optimization for Dynamic Precision Scaling in DSP Systems," *Proceedings of the IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Istanbul, Turkey, November 2013.

C52. S. Chakravarty, Z. Zhao, A. Gerstlauer, **[40%/30%/30%]** "Automated, Retargetable Back-Annotation for Host Compiled Performance and Power Modeling," *Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Montreal, Canada, October 2013.

C51. A. Mariano, D. Lee, A. Gerstlauer, D. Chiou, **[40%/30%/20%/10%]** "Hardware and Software Implementations of Prim's Algorithm for Efficient Minimum Spanning Tree Computation," *Proceedings of the International Embedded Systems Symposium (IESS)*, Paderborn, Germany, June 2013.

C50. H. Park, A. Gerstlauer, **[70%/30%]** "Toward a Fast Stochastic Simulation Processor for Biochemical Reaction Networks," *Proceedings of the IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, Washington, DC, June 2013.

C49. A. Pedram, J. McCalpin, A. Gerstlauer, **[50%/40%/10%]** "Transforming A Linear Algebra Core to An FFT Accelerator," *Proceedings of the IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, Washington, DC, June 2013.

C48. P. Razaghi, A. Gerstlauer, **[70%/30%]** "Multi-Core Cache Hierarchy Modeling for Host-Compiled Performance Simulation," *Proceedings of the Electronic System Level Synthesis Conference (ESLSyn)*, Austin, TX, June 2013.

C47. D. Pfeifer, A. Gerstlauer, J. Valvano, **[60%/20%/20%]** "Dynamic Resolution in Distributed Cyber-Physical System Simulation," *Proceedings of the ACM SIGSIM Conference on Principles of Advanced Discrete Simulation (PADS)*, Montreal, Canada, May 2013.

C46. A. Pedram, A. Gerstlauer, R. van de Geijn, **[70%/20%/10%]** "Floating Point Architecture Extensions for Optimized Matrix Factorization," *Proceedings of the 21st IEEE International Symposium on Computer Arithmetic (ARITH21)*, Austin, TX, April 2013.

C45. K. He, A. Gerstlauer, M. Orshansky, **[40%/30%/30%]** "Low-Energy Digital Filter Design Based on Controlled Timing Error Acceptance," *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, San Jose, CA, March 2013.

C44. J. Miao, K. He, A. Gerstlauer, M. Orshansky, **[40%/10%/20%/30%]** "Modeling and Synthesis of Quality-Energy Optimal Approximate Adders," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, pp. 728-735, November 2012.

C43. J. W. Massey, J. Starr, S. Lee, D. Lee, A. Gerstlauer, R. W. Heath, **[30%/10%/30%/10%/10%/10%]** "Implementation of a Real-Time Wireless Interference Alignment Network," *Proceedings of the Asilomar Conference on Signals, Systems and Computers (ACSSC)*, Pacific Grove, CA, pp. 104-108, November 2012.

C42. D. Lee, H. Park, A. Gerstlauer, **[40%/30%/30%]** "Synthesis of Optimized Hardware Transactors from Abstract Communication Specifications," *Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Tampere, Finland, pp. 403-412, October 2012.

C41. A. Pedram, A. Gerstlauer, R. A. van de Geijn, **[70%/20%/10%]** "On the Efficiency of Register File versus Broadcast Interconnect for Collective Communications in Data-Parallel Hardware Accelerators," *Proceedings of the IEEE/IFIP International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*, New York, NY, pp. 19-26, October 2012.

C40. A. Pedram, S. Z. Gilani, N. S. Kim, R. van de Geijn, M. Schulte, A. Gerstlauer, **[35%/10%/10%/10%/10%/25%]** "A Linear Algebra Core Design for Efficient Level-3 BLAS," *Proceedings of the IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, Delft, The Netherlands, pp. 149-152, July 2012.

C39. K. He, A. Gerstlauer, M. Orshansky, **[40%/30%/30%]** "Low-Energy Signal Processing using Circuit-Level Timing-Error Acceptance," *Proceedings of the IEEE International Conference on Integrated Circuit Design and Technology (ICICDT)*, Austin, TX, 4 pages, May 2012.

C38. A. Gerstlauer, S. Chakravarty, M. Kathuria, P. Razaghi, **[25%/25%/25%/25%]** "Abstract System-Level Models for Early Performance and Power Exploration," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Sydney, Australia, pp. 213-218, January 2012.

C37. P. Razaghi, A. Gerstlauer, **[70%/30%]** "Automatic Timing Granularity Adjustment for Host-Compiled Software Simulation," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Sydney, Australia, pp. 567-572, January 2012.

C36. D. Pfeifer, A. Gerstlauer, **[80%/20%]** "Expression-Level Parallelism for Distributed Spice Circuit Simulation," *Proceedings of the IEEE/ACM International Symposium on Distributed and Real Time Applications (DS-RT)*, Manchester, United Kingdom, pp. 12-17, September 2011.

C35. M. S. Lopez, A. Gerstlauer, A. Avila, S. O. Martinez-Chapa, **[60%/20%/10%/10%]** "A Programmable and Configurable Multi-port System-on-Chip for Stimulating Electrokinetically-Driven Microfluidic Devices," *Proceedings of the International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, Boston, MA, pp. 8361-8364, September 2011.

C34. A. Abdel-Hadi, J. Michel, A. Gerstlauer, S. Vishwanath, **[40%/30%/20%/10%]** "Real-Time Optimization of Video Transmission in a Network of AAVs," *IEEE Vehicular Technology Conference (VTC)*, San Francisco, CA, 5 pages, September 2011.

C33. A. Pedram, A. Gerstlauer, R. A. van de Geijn, **[40%/30%/30%]** "A High-Performance, Low-Power Linear Algebra Core," *Proceedings of the IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, Santa Monica, CA, pp. 35-42, September 2011.

C32. J. Lin, A. Srivatsa, A. Gerstlauer, B. L. Evans, **[40%/20%/30%/10%]** "Heterogeneous Multiprocessor Mapping for Real-Time Streaming Systems," *Proceedings of the IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, Prague, Czech Republic, pp. 1605-1608, May 2011.

C31. P. Razaghi, A. Gerstlauer, **[60%/40%]** "Host-Compiled Multicore RTOS Simulator for Embedded Real-Time Software Development," *Proceedings of the Design, Automation and Test in Europe (DATE) Conference*, Grenoble, France, 6 pages, March 2011.

C30. K. He, A. Gerstlauer, M. Orshansky, **[40%/30%/30%]** "Controlled Timing-Error Acceptance for Low Energy IDCT Design," *Proceedings of the Design, Automation and Test in Europe (DATE) Conference*, Grenoble, France, 6 pages, March 2011.

C29. R. Dömer, W. Chen, X. Han, A. Gerstlauer, **[30%/30%/30%/10%]** "Multi-Core Parallel Simulation of System-Level Description Languages," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Yokohama, Japan, pp. 311-316, January 2011.

C28. J. Gladigau, A. Gerstlauer, C. Haubelt, M. Streubühr, J. Teich, **[30%/20%/20%/30%/0%]** "A System-Level Synthesis Approach from Formal Application Models to Generic Bus-Based MPSoCs," *Proceedings of the IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS)*, Samos, Greece, pp. 118-125, July 2010.

C26. A. Gerstlauer, G. Schirner, **[90%/10%]** "Platform Modeling for Exploration and Synthesis," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Taipei, Taiwan, pp. 725-731, January 2010.

C25. G. Schirner, A. Gerstlauer, R. Dömer, **[60%/20%/20%]** "System-Level Development of Embedded Software," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Taipei, Taiwan, pp. 903-909, January 2010.

C24. A. Pedram, D. Craven, A. Gerstlauer, **[40%/30%/30%]** "Modeling Cache Effects at the Transaction Level," *Analysis, Architectures and Modeling of Embedded Systems*, Proceedings of the IFIP International Embedded Systems Symposium (IESS), Langenargen, Germany, edited by Achim Rettberg, Mauro Zanella, Michael Amann, Michael Keckeisen, Franz Rammig, vol. 310 of IFIP Advances in Information and Communication Technology, Springer, ISBN 978-3-642-04283-6, pp. 89-101, September 2009.

C23. A. Banerjee, A. Gerstlauer, **[70%/30%]** "Transaction Level Modeling of Best-Effort Channels for Networked Embedded Devices," *Analysis, Architectures and Modeling of Embedded Systems*, Proceedings of the IFIP International Embedded Systems Symposium (IESS), Langenargen, Germany, edited by Achim Rettberg, Mauro Zanella, Michael Amann, Michael Keckeisen, Franz Rammig, vol. 310 of IFIP Advances in Information and Communication Technology, Springer, pp. 77-88, ISBN 978-3-642-04283-6, September 2009.

C22. R. Dömer, A. Gerstlauer, W. Mueller, **[45%/10%/45%]** "Introduction to Hardware-Dependent Software Design," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Yokohama, Japan, pp. 290-292, January 2009.

ANDREAS GERSTLAUER
Works Forthcoming

In the following, papers that have been accepted but not yet published are listed. Paper indices refer back to the full publication list in my CV. Copies of acceptance letters for conference papers are attached.

A. Refereed Archival Journal Publications

J12. D. Pfeifer, J. Valvano, A. Gerstlauer, "SimConnect and SimTalk for Distributed Cyber-Physical System Simulation," *Simulation: Transactions of the Society for Modeling and Simulation International*, accepted for publication, November 2012.
Pre-print published online March 5, 2013: http://dx.doi.org/10.1177/0037549712472755

B. Refereed Conference Proceedings

C54. J. Miao, A. Gerstlauer, M. Orshansky, "Approximate Logic Synthesis under General Error Magnitude and Frequency Constraints," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, November 2013.

C53. S. Lee, A. Gerstlauer, "Fine Grain Word Length Optimization for Dynamic Precision Scaling in DSP Systems," *Proceedings of the IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Istanbul, Turkey, November 2013.

C52. S. Chakravarty, Z. Zhao, A. Gerstlauer, "Automated, Retargetable Back-Annotation for Host Compiled Performance and Power Modeling," *Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Montreal, Canada, October 2013.

J 12

Subject: Re: ACTION REQUIRED: Simulation: Transactions of the Society for Modeling and Simulation International Contributor Form
From: Dylan Pfeifer <dcpfeifer@gmail.com>
Date: 11/14/2012 9:56 AM
To: "Jonathan W. Valvano" <Jonathan.Valvano@engr.utexas.edu>, "Andreas M Gerstlauer" <gerstl@ece.utexas.edu>

Thought you might like to see this!!

On Nov 14, 2012 9:44 AM, <vmpate@scs.org> wrote:

14-Nov-2012
Dear Mr. Dylan Pfeifer,

Your manuscript "SimConnect and SimTalk for Distributed Cyber-Physical System Simulation" has been accepted for publication in Simulation: Transactions of the Society for Modeling and Simulation International.

In order for SAGE to proceed with publication of your article, you must complete a Contributor Form. Under the agreement, you retain copyright to your work and grant an exclusive license to SAGE to publish the article.

You should review and complete the form online at the journal's SAGETRACK site. The following link will take you there directly.

http://mc.manuscriptcentral.com/simulation?URL_MASK=HCbMRCDR8j2ftwTtNMmx

Please note that without a completed agreement, we are unable to proceed with publication of your article.

If you have any questions please contact the Editorial Office.

With best wishes,
Vicki Pate
vmpate@scs.org
Simulation: Transactions of the Society for Modeling and Simulation International Editorial Office

C54

Subject: ICCAD 2013 Notification of Acceptance for paper 365
From: ICCAD 2013 <iccad2013@easychair.org>
Date: 6/21/2013 2:11 AM
To: Andreas Gerstlauer <gerstl@ece.utexas.edu>

Dear Andreas,

Congratulations!! On behalf of the ICCAD TPC, we are pleased to inform you that your paper entitled

Approximate Logic Synthesis under General Error Magnitude and Frequency Constraints

has been selected for publication in the ICCAD'13 technical program.

This year we received 354 final submissions from all over the world, a 5% increase from last year. After a rigorous double-blind review process that culminated in a full-day face-to-face meeting of the entire technical program committee at Austin, Texas, only 92 regular papers were selected for inclusion, making the acceptance rate of only 26%.

Please see reviewer's comments below. We hope that you will find them helpful in preparing your final paper for publication. Guidelines for preparing your final paper and presenting at the conference will be sent in a separate email; they will also be available at the ICCAD web site: http://www.iccad.com by June 24 (next Monday).

Thank you so much for your excellent work. We are looking forward to seeing you at ICCAD'13 in San Jose, November 18-21, 2013! We also hope to receive your submissions to ICCAD'14 next April!!

Best regards,

Yao-Wen Chang (ICCAD'13 Program Chair; ywchang@cc.ee.ntu.edu.tw)

Diana Marculescu (ICCAD'13 Vice Program Chair; dianam@cmu.edu)

---------- REVIEW 1 ----------
PAPER: 365
TITLE: Approximate Logic Synthesis under General Error Magnitude and Frequency Constraints
AUTHORS: Jin Miao, Andreas Gerstlauer and Michael Orshansky

OVERALL EVALUATION: 0 (borderline paper)

---------- REVIEW ----------
The authors propose an ALS approach considering both the magnitude and frequency of errors. For this purpose, they follow a two step approach. First the magnitude constraints are solved by relating the problem to Boolean relation minimization. The obtained solution is then further optimized such that the frequency constraints are met.

The approach is interesting and its efficiency is demonstrated by the experiments that have been performed (although not many benchmarks have been considered). However, the main concern with the paper lies in the formalization which is often not consistent and vague, such that it is hard to really reconsider all steps or validate whether the theorems are correctly proven. Examples:

- The definition of F-F_m to constrain the magnitude error is not clear

- It seems that the use of M and m and R and r is sometimes mixed up, in particular

when used together with F, i.e. F_m vs F_M, and F_r vs F_R

- When the difference F-F_m is first defined it is not clear whether output pattern or bits are counted. This gets clear in (1). But I cannot relate Example 2.1 to F-F_m.

- The proof for Theorem 3.1 is trivial, but there is no proof for Theorem 3.2

- In Example 3.1 and in Definition 3.6 variables are primed. What does that mean?

- In Eq. (8) and (11) I do not understand the sum notation. What is the index variable? What is the precise range?

Minors:

- page 4: Equation 5 -> Equation (5)

- Last Theorem in Sect. 3 has no number

---------- REVIEW 2 ----------
PAPER: 365
TITLE: Approximate Logic Synthesis under General Error Magnitude and Frequency Constraints
AUTHORS: Jin Miao, Andreas Gerstlauer and Michael Orshansky

OVERALL EVALUATION: 0 (borderline paper)

---------- REVIEW ----------
In this paper, the authors propose an approximate logic synthesis algorithm considering error magnitude and frequency constraints. The proposed method contains two phases. The first phase generates a minimum cover under error magnitude constraint, while the second phase tries to fit the frequency constraint with least literal increment. The authors transform the first phase to the Boolean relations minimization problem. Then, they adopt iterative refinement for the second phase.

I have the following comments/questions.
1) Although the title says this work considers magnitude and frequency constraints together, this paper still solves these two constraints in two phases. Is it possible to simultaneously consider these two constraints?
2) No comparison with state-of-the-art works is provided. Although previous work does not consider magnitude and frequency constraints together, it would be nice if the authors can compare the first phase with existing works.
3) In (4), F_M should be F. Otherwise, the magnitude constraint might not be satisfied. Besides, because F_M is given for the second phase, L(F_M) can be removed from the objective function.
4) Sorting the cost with respect to DIFF primes is a clever idea.

---------- REVIEW 3 ----------
PAPER: 365
TITLE: Approximate Logic Synthesis under General Error Magnitude and Frequency Constraints
AUTHORS: Jin Miao, Andreas Gerstlauer and Michael Orshansky

OVERALL EVALUATION: 1 (weak accept)

---------- REVIEW ----------
This paper addresses the problem of approximate logic synthesis (ALS). ALS is to synthesize a minimum-cost approximate Boolean network whose behavior deviates in a well-defined manner from a specified exact Boolean function. Here, the deviation is to be constrained by both the magnitude and frequency of the error.
The authors make two contributions in solving this general ALS problem:
(1) they establish that the approximate synthesis problem un-constrained by the frequency of errors is isomorphic with the Boolean relations (BR) minimization problem.

That equivalence allows to exploit recently developed fast algorithms for BR problems to solve the error magnitude-only constrained ALS problem.
(2) They propose an efficient heuristic algorithm for iterative refining the magnitude-constrained solution to achieve the error frequency constraint.

The authors propose a two-level logic minimization algorithm that synthesizes a minimum-cost cover of a Boolean function that is allowed to deviate from an exact Boolean function in a constrained manner. The first phase solves the problem that is constrained only by magnitude of error. In the second phase, this frequency unconstrained problem is iteratively refined to arrive at a solution that also satisfies the original error frequency constraint.

The proposed algorithm is capable of synthesizing approximate circuits for arbitrarily specified error deviations, and is most immediately applicable to arithmetic blocks, for which experiments demonstrate the effectiveness in achieving significantly reduced literal counts across a wide range of flexible error frequency and magnitude constraints.

This is an interesting paper addressing an important problem. A more interesting would be finding multi-level realizations which optimize energy efficiency. As it is, it is a step in the right direction, but not a complete solution to a practical problem.

The paper is clearly written.

---------- REVIEW 4 ----------
PAPER: 365
TITLE: Approximate Logic Synthesis under General Error Magnitude and Frequency Constraints
AUTHORS: Jin Miao, Andreas Gerstlauer and Michael Orshansky

OVERALL EVALUATION: 2 (accept)

---------- REVIEW ----------
The paper is about synthesis of approximate logic functions: they different in "magnitude" by only a fixed amount versus the original exact function, and moreover, there is a limit on the # of min terms that are in error.

First, the authors show that the error magnitude minimization can be handled as a Boolean relations problem. They solve that, and refine the solution greedily to find a function that, while minimizing the # literals increased, meets the constraint on the # of minterms that are in error.

I like the paper and it is quite clear. The work is pretty novel and this is a good area for research.

A few comments:

The error frequency constraint: shouldn't this be based on typical input vectors to the function? i.e. what if one wants to specify that, under typical input vectors, the function should produce an erroneous solution in at most X% of the cases.

A significant issue is that the experiments don't consider any REAL examples? it's just simple adders and multipliers. Why can't a signal processing application be considered? say, at least an FIR filter?

Significant issue with this paper is the scalability: even for the simple adders and multipliers, some of the run-times for the approach are in minutes or HOURS. It makes me wonder whether this can be applied to REAL cases?

The authors seem not to have synthesized their circuits: so the area/speed/power benefits of the approximate circuits are not presented. Rather, the benefits shown are "indirect".

C53

Subject: acceptance letter for your submission to VLSI-SOC 2013
From: VLSI-SoC 2013 <vlsisoc2013@easychair.org>
Date: 6/13/2013 1:22 PM
To: Andreas Gerstlauer <gerstl@ece.utexas.edu>

Dear authors(Seogoo Lee and Andreas Gerstlauer),

on behalf of the VLSI-SOC 2013 Program Committee, we are delighted to inform you that the following submission has been accepted as a regular paper for the conference:

170 : Fine Grain Word Length Optimization for Dynamic Precision Scaling in DSP Systems

This year we had a very competitive process, with more than 235 confirmed submissions, with an acceptance rate of less than 20% for regular papers, and less than 28% when short papers are included. Your paper went through a very careful and detailed review, and we are glad it made to the final selected list.

While preparing your final version for submission, please carefully consider the Program Committee comments on how to improve your article. As a regular paper, you are allowed 6 pages in the conference proceedings and a 25 minutes slot (20 minutes for presentation plus 5 for questions) to present your work.

To upload your final manuscript, please visit the easychair site. The deadline for final paper submission is July 1st, 2013.

Additional instructions concerning copyright and registration will follow soon.

If you have any additional questions, please feel free to contact us.

Thank you for your contribution to VLSI-SOC 2013

Alex Orailoglu and Luigi Carro
VLSI-SOC 2013 Program co-chairs

C52

Subject: Fwd: Your CODES+ISSS 2013 Submission (Number 125)
From: Zhuoran Zhao <zhuoran@utexas.edu>
Date: 7/2/2013 1:18 PM
To: Andreas Gerstlauer <gerstl@ece.utexas.edu>, Suhas Chakravarty <suhas.chakravarty@gmail.com>

Just received the reviews for the CODESISSS paper..

---------- Forwarded message ----------
From: <panda@cse.iitd.ac.in>
Date: Tue, Jul 2, 2013 at 1:02 PM
Subject: Your CODES+ISSS 2013 Submission (Number 125)
To: zhuoran@utexas.edu

Dear Mr. Zhuoran Zhao,

Congratulations! We are pleased to inform you that your paper submission titled:

Automated, Retargetable Back-Annotation for Host
Compiled Performance and Power Modeling

was accepted for presentation at CODES+ISSS 2013. The papers were evaluated by the Technical Program Committee, and 31 papers were finally selected from 111 submissions, resulting in a 27.9% acceptance ratio. The conference Program Committee recognizes that your paper makes a significant contribution to the field. The Program Committee has worked hard to ensure that useful feedback is given to the authors. The reviews for your paper are attached.

Please understand that at least one author needs to register for the conference and attend the conference to present the paper. Each paper will be allotted 30 minutes comprising a formal presentation of 25 minutes followed by a 5 minute interaction with the audience. In order to interact with a wider audience, the presenter is also expected to put up a poster on the research immediately following the technical session. Information about the schedule of the technical sessions will be up on the CODES+ISSS web site soon.

The final version of your manuscript is due on 26 July 2013. Detailed information about preparing the final version, posters, registration, and visa invitation letters will be sent to you separately.

We thank your for your valuable contribution to CODES+ISSS 2013, and look forward to meeting you at Montreal in September/October.

Best Regards,
Radu Marculescu and Preeti Ranjan Panda
CODES+ISSS 2013 TPC Chairs

==========
CODES+ISSS 2013 Reviews for Submission #125
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Title: Automated, Retargetable Back-Annotation for Host Compiled Performance and Power

Modeling

Authors: Suhas Chakravarty, Zhuoran Zhao and Andreas Gerstlauer

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REVIEWER #1

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Reviewer's Scores

Overall: 4
Reviewer confidence: 2
Novelty: 4
Usefulness: 4
Writing and figure quality: 5

Comments

This paper describes an approach for improving the accuracy of timing and energy estimations given by host-compiled code. The authors claim that this approach is relatively easy to adapt to different target hardware architectures. The approach works through back-annotation of pairs of basic
blocks of the source code with values from an instruction set simulator and an energy analysis tool. Several variations of the proposed simulation approach are compared to a traditional combination of an instruction set simulator and an energy analysis tool. The results show that the proposed approach speeds up simulation in some cases while providing good timing and energy accuracy.

In general, this paper was well written and clearly explained the proposed technique, the experiments, and the results. The only major drawback of this paper is that the proposed approach was only compared to a traditional instruction set simulator. The authors discuss a number of other existing approaches to the problems being addressed in this paper, yet the proposed approach isn't compared to any of them. Thus, it could be argued that some of the claims in the related work section about the drawbacks of existing approaches are subjective and unsupported by experimental evidence.

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REVIEWER #2

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Reviewer's Scores

Overall: 4
Reviewer confidence: 2
Novelty: 3
Usefulness: 4
Writing and figure quality: 4

Comments

Paper builds on a previous effort of back-annotation for retarget able power and performance estimation. In this work an automated methodology is outlined, in which the compiler generated IR is annotated with timing and energy information. In addition the CDFG is constructed from the IR, which may lead to inconsistencies as compared to the binary due to compiler optimization. Methodology
additionally incorporates a heuristic subgraph mapping algorithm that utilizes debug information to alleviate this problem. In addition, the block characterization through pairwise execution seems to be one of the main factors in terms of obtaining a better estimation. An ISS and McPAT are utilized to determine the annotation values.

Overall, the paper is well written and easy to follow. The results show promising
energy and timing estimations.

Paper mentions that the higher estimation errors were isolated combinations due to multi-level block dependencies. Is there any analysis on the level of these dependencies and the tradeoffs to performing multilevel characterization to determine the annotation values?

Paper also mentions that future work will evaluate energy consumption based on actual data flowing through blocks. What data set was utilized in the current framework
evaluation and what impact do you anticipate by changing these sets?

While the estimate error was relatively low, paper mentions the use of heuristics
to build the CDFG. Is there any analysis in the resulting CDFG, in particular does
this structure contribute to the error or is there some other underlying factor such as McPAT that leads to the bulk of inaccuracies?

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REVIEWER #3

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Reviewer's Scores

Overall: 2
Reviewer confidence: 2
Novelty: 2
Usefulness: 4
Writing and figure quality: 5

Comments

The paper is well written, and clearly points out methodology ideas, advantages and issues. Moreover, several possible future works are reported. State of the art is well analyzed. Some reference could be reported in the introduction to confirm the reported considerations.

Experiments are good, and results are well analyzed.

My main concern is related to the novelty of the approach w.r.t [26].
The authors claim that the proposed work is based on a previous work [26] whose reference details are omitted for blind review. Anyway, it was not difficult to go back to paper [26] with google.
[26] is "Abstract System-Level Models for Early Performance and Power Exploration" presented at ASP-DAC 2012.
The authors say that w.r.t [26] the main contributions of the current paper are:
1- automation of the flow
2- fully support of compiler optimizations
3- details about the pairwise block characterization
4- extension of original concept with a binary-to-IR mapping algorithm and accurate block characterization.

My opinion is:
1- contribution 1 is not so scientifically relevant since it appears to be only an implementation aspect;
2- this part is effectively new;
3- details are appreciated, but it seems no new contribution are provided;
4- this is an improvement w.r.t [26], however since experimental results in the current paper and in [26] are different, it is not possible to compare and evaluate the effect of the improvement.

Nothing bad, but the impression is that the current work is "only" an extended version of [26].

>From the methodology point of view some observations are:
- It is not clear if the block matching algorithm always produces the correct match, or whether there are cases where it fails, since it seems based on a heuristic.

- Probably, the main limit of this approach is the analysis phase, which is quite time consuming. Actually back annotation is a one-time effort, but only as long as the design is not changed... it is likely that the design is changed during refinement phases. Indeed one of the objectives of power and timing estimation is to have feedbacks to better optimize the design.

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REVIEWER #4

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Reviewer's Scores

Overall: 3
Reviewer confidence: 2
Novelty: 2
Usefulness: 3
Writing and figure quality: 4

Comments

The paper is well written, most concepts are comprehensibly explained, and the figures are well done.

1) Main Weakness: The novelty of this paper is questionable.
Cf. Section 1.1, last paragraph: "An overview of our basic flow for retargetable power and performance back-annotation was first introduced in [26]. However, in earlier work, the flow was not automated, compiler optimizations were not fully supported and no details about the pairwise block characterization were presented. In this paper, we extend the original concept with a binary-to-IR mapping algorithm and accurate block characterization to provide a fully automated flow that supports complex optimized code."

The only actual novelty is the automated mapping between IR and binary CFGs. Compiler optimizations are taken into account implicitly by extracting timing and power information from the binary representation. And the concept of pairwise block characterization itself is no novel contribution, only the presentation of the details.

Several mentions of unfinished work left for the future, highlight the lack of novelty:

2.1: "Building the CFG for the binary follows a similar process, but it requires identifying all assembly instructions that can cause flow changes." [...] "This can be mitigated, however,

by automatically extracting the knowledge of control flow change instruction from the ADL description of the processor, which we plan to address in future work."

2.2.2: "Dynamic branch predictors are not accurately characterized using our approach. To generally capture dynamic effects, our back-annotated model can be augmented with dynamic cache and branch predictor simulation models from literature. Such extensions with existing work are, however outside the scope of the paper."

2.2.3: "Switching activity and hence power consumption of code block will generally be data (input) dependent. We currently annotate a single energy consumption figure (based on default McPat activity factors) per pair of basic blocks, leading to small residual errors in our current flow. In future work, we plan to develop an input-dependent characterization of the per-block energy consumption based on the actual data flowing through the block during simulated execution."

2) Shortcomings of the actual novel contribution:
While the pairwise execution is presented in a very detailed (to some degree almost unnecessarily detailed), manner, the explanation of the mapping algorithm, the actual novelty, falls a bit short:

In the description of Algorithm 2, the purpose of the Powersets of succeeding nodes, is not immediately obvious. This also holds for the metric of the cost function. The correspondence between the local cost / replacing succeeding nodes (elements of the Powersets) with their succeeding nodes and the mismatches in the two CFGs should be made clarified.

The quadratic complexity of the over all mapping is doubtful. There are three nested loops in the cost function: two ranging over powersets (2^|N|) and one over each possible bijection (N!). The complexity of the algorithm therefore should be elaborated in detail.

3) Small issues with the Algorithm:
The function MAPPING (Alg. 2) simply returns a cost for comparing two nodes. It thus is only a cost function, which can be a part of a Mapping algorithm. Line 17: "if |SS1| == |SS1| then" the right hand side probably should be "|SS2|".

4) Evaluation:
The proposed solution only makes sense if the inputsets of the benchmarks are sufficiently large. As the time spent for BA is significant in all other cases, the sizes of the CFGs in the benchmarks would be interesting. Same goes Section 1: "Automated one-time back-annotation of code is fast (on the order of 1-2 minutes)", which raises the question for what size of application?

5) remarks:

1.1 Related work: "We have found debug information of optimized code to be unreliable. We therefore implement an approach that combines a flow graph matching algorithm with debug information as fall back." Why fall back to an unreliable solution?

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REVIEWER #5

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Reviewer's Scores

Overall: 3
Reviewer confidence: 3
Novelty: 2
Usefulness: 3
Writing and figure quality: 4

Comments

The main contribution of this paper is to propose a fast and accurate host-compiled simulation approach for automated and retargetable modeling of both performance and power consumption leveraging existing, open-source architecture description language (ADL). A heuristic subgraph matching algorithm is used to map basic blocks to in the intermediate representation to binary code.

The major concern about the paper is the lack of details to highlight its novelty compared to [26]. Majority of 10 pages describes well understood concepts in compiler and ADL domain. Figure 1 is almost identical to Figure 2 of [26]. Ideally, the paper should have focused on presenting technical details compared to [26]. For example, there is no comparison compared to [26]. In fact, there is no comparison compared to any of the existing state-of-the-art approaches. There is no discussion about the following paper unless it is [26]. Arguably, [26] outlined some of the contributions claimed in this paper.

Andreas Gerstlauer, Suhas Chakravarty, Manan Kathuria, and Parisa Razaghi, "Abstract System-Level Models for Early Performance and Power Exploration", ASPDAC 2012.

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No leaves without pay taken.

ANDREAS GERSTLAUER
Statistical Summary for In-Rank

Peer-reviewed Journal Publications	9
Peer-reviewed Conference Publications	32
Corresponding Author on Peer-Reviewed Publications	4 (3 invited)
Total Citations of all Publications (career)*	2135
h-index (career)*	21
Total Research Funding	$2.17M
Candidate Share Research Funding	$1.39M
Total Number of Grants/Contracts Received	13
Number of Grants/Contracts Received as PI	10
PhD Students Completed †	1.5
MS Students Completed †	7.5
PhD Students in Pipeline (as of 09/2013) †	6
MS students in Pipeline (as of 09/2013) †	2
Courses Taught	11
Weighted Average UG Course GPA	3.04
# of Students Taught	409
Average Instructor Evaluation UG	4.10
Average Instructor Evaluation Grad	4.23
Average Course Evaluation UG	3.74
Average Course Evaluation Grad	3.79
Teaching Awards	0
Student Organizations Advised	2
Undergraduates Supervised	11
Department Committees and Service	9
Cockrell School Committees	0
University Committees and Service	0
Journal Editorial Boards	2
Journal Reviews/Number of Journals	34 / 13
Symposia Organized	4
Invited Talks	33

* Source:
- ☒ Publish or Perish
- ☐ ISI Web of Knowledge

† Counted as 1 if sole advisor, 0.5 if co-advised

SUMMARY OF ACTIVITIES FOR
ANDREAS GERSTLAUER
September 1, 2010 – August 31, 2011

A. Research:

1. Awards and Honors

N/A

2. Invited Addresses and Colloquia

- "Using Cutting-Edge Tools for Communication System Design," National Instruments NIWeek conference, Austin, TX, August 2011.
- "System-Level Design of Heterogeneous Embedded Multi-Core Platforms," Department of Informatics, University of Tübingen, Germany, June 2011.
- "Low Power, High Performance Linear Algebra Processing," IBM Austin Research Lab, Austin, Texas, May 2011.
- "System-Level Design of Heterogeneous Embedded Multi-Core Platforms," Huawei Technologies USA, Dallas, Texas, March 2011.
- "Embedded System Design Challenges and Trends," Texas Instruments, Dallas, Texas, March 2011.
- "Embedded Systems Research," 3M, Austin, Texas, January 2011.
- "System-Level Design of Multi-Processor/Multi-Core Systems-on-Chip," Intel Research, Hillsboro, Oregon, November 2010.
- "System-Level Design for Heterogeneous Low-Power and High-Performance Compute Fabrics," National Instruments, Austin, Texas, October 2010.

3. Publications

(a) Journals and books
Indicate published, accepted for publication, revised or submitted and under review.

- K. He, A. Gerstlauer, M. Orshansky, "Circuit-Level Timing Error Acceptance for Low-Energy Image Processing," *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, submitted, August 2011.
- P. Razaghi, A. Gerstlauer, "Predictive OS Modeling for Host-Compiled Simulation of Periodic Real-Time Task Sets," *IEEE Embedded System Letters*, submitted, July 2011.
- J. Gladigau, A. Gerstlauer, C. Haubelt, M. Streubühr, J. Teich, "Automatic System-Level Synthesis: From Formal Application Models to Generic Bus-Based MPSoCs," *Transactions on High-Performance Embedded Architectures and Compilers (Transactions on HiPEAC)*, accepted for publication, May 2011.

(b) Refereed Conference Proceedings
Indicate published or accepted for publication.

- D. Pfeifer, A. Gerstlauer, "Expression-Level Parallelism for Distributed Spice Circuit Simulation," *Proceedings of the IEEE/ACM International Symposium on Distributed and Real Time Applications (DS-RT)*, accepted for publication, July 2011.
- M. S. Lopez, A. Gerstlauer, A. Avila, S. O. Martinez-Chapa, "A Programmable and Configurable Multi-port System-on-Chip for Stimulating Electrokinetically-Driven Microfluidic Devices," *Proceedings of the International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, accepted for publication, July 2011.
- A. Abdel-Hadi, J. Michel, A. Gerstlauer, S. Vishwanath, "Real-Time Optimization of Video Transmission in a Network of AAVs," *IEEE Vehicular Technology Conference (VTC)*, accepted for publication, July 2011.
- A. Pedram, A. Gerstlauer, R. van de Geijn, "A High-Performance, Low-Power Linear Algebra Core," *Proceedings of the IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, accepted for publication, July 2011.
- J. Lin, A. Srivatsa, A. Gerstlauer, B. Evans "Heterogeneous Multiprocessor Mapping for Real-time Streaming Systems," *International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, Prague, Czech Republic, May 2011.
- P. Razaghi, A. Gerstlauer, "Host-Compiled Multicore RTOS Simulator for Embedded Real-Time Software Development," *Design, Automation and Test in Europe (DATE)*, Grenoble, France, March 2011.
- K. He, A. Gerstlauer, M. Orshansky, "Enabling Improved Quality-Energy Tradeoff for Low Energy IDCT Architecture," *Design, Automation and Test in Europe (DATE)*, Grenoble, France, March 2011.
- R. Dömer, W. Chen, X. Han, A. Gerstlauer, "Multi-Core Parallel Simulation of System-Level Description Languages," *Proceedings of the Asia and South Pacific Design Automation Conference (ASPDAC)*, Yokohama, Japan, January 2011. (invited paper)

(c) Conference Presentations Without Proceedings of Full Papers

N/A

3. Student Advising

(a) Completed PhD Theses

Names of students and program (e.g. ECE, CS, Physics, etc.)

- Martha Salome Lopez De La Fuente, "Definition, Design and Implementation of a Processor-Based Stimulation System for Eletrokinetically-Driven Fluidic Devices," Information Technologies and Communications, Monterey Institute of Technology, Monterey, Mexico, May 11, 2011. (external co-advisor with Prof. Sergio O. Martinez Chapa)

(b) Current Graduate Advisees

PhD:

- Parisa Razaghi
- Hyungman Park
- Dongwook Lee
- Ardavan Pedram (with Robert van de Geijn, CS)
- Ku He (with Michael Orshansky)

- Jin Miao (with Michael Orshansky)
- Ahmed Abdel Hadi (with Sriram Vishwanath)
- Wei-Chen Su

MS:

- Suhas Chakravarty
- Manan Kathuria

Number of graduate students supported by grants, 2010-11	Number of graduate students supported by grants, 2011-12 (*anticipated*)	Number of Ph.D. advisees supported as T.A., Fellow, etc., 2010-11	Number of Ph.D. advisees supported as T.A., Fellow, etc., 2011-12 (*anticipated*)
3	5	1	1

4. Current Research Projects and Grants

Title, agency, PI, role, amount, duration
Also list active research projects that are not funded (e.g. carried out by PhD level students)

- A. Gerstlauer (PI), "Compiler-Assisted MPSoC Assembly and Mapping," Unrestricted, no-overhead gift, Intel Labs, Santa Clara, $46,000, 9/2010-8/2011.
- A. Gerstlauer (PI), M. Orshansky, "Formal Synthesis of Low-Energy Signal Processing Systems Relying on Controlled Timing-Error Acceptance," National Science Foundation (NSF), Grant CCF-1018075, $449,676, 9/2010-8/2013.
- A. Gerstlauer (PI), "Automatic Platform Model Calibration and Tuning," Semiconductor Research Corporation (SRC), Contract 2010-HJ-2085, $255,000, 8/2010-7/2013.
- "Towards Enabling Full−Cell Biochemical Network Simulations," Summer Research Assignment (SRA), 6/2011-7/2011, $20,000.
- A. Gerstlauer, "Host-Compiled Multi-Core Software Simulation"
- A. Gerstlauer, S. Vishwanath, "Horus: A Testbed for Wireless UAV Networks"

5. Proposal Submissions

Title, agency, PI, role, amount, duration

- A. Gerstlauer (PI), Lizy John, "PERPTET: Design Exploration Tools for Heterogeneous Multicores," Semiconductor Research Corporation (SRC), $399,000, 1/2012-1/2014
- A. Gerstlauer (PI), H. Vikalo, „ ABI Innovation: Stochastic In-Silico Simulation System for Genetic Regulatory Network Modeling and Inference," National Science Foundation, $489,592, 1/2012-12/2014
- A. Gerstlauer (PI), "High-Performance and Low-Power Compute Fabrics for Linear Algebra Processing," Department of Energy (DOE), Early Career Research Program (ECRP), $751,949, 6/2011-5/2016.
- A. Gerstlauer (PI), R. van de Geijn, J. Abraham, E. Swartzlander, "SHF:Large:Hardware/Software Foundations for Low Power and High Performance Linear Algebra Computing," National Science Foundation, $1,545,847, 8/2011-7/2014.
-

B. <u>Teaching</u>

6. Special Projects, Lab and Course Developments, etc.

C. Service Activities

7. University Service
Departmental and university-wide committees etc.

- Graduate Admissions Committee, Computer Engineering/Computer Architecture and Embedded Processors, ECE Department
- Graduate Admissions Committee, Integrated Circuits and Systems, ECE Department
- Curriculum Committee, Computer Engineering/Computer Architecture and Embedded Processors, ECE Department
- Curriculum Committee, Integrated Circuits and Systems, ECE Department
- Faculty Committee, Computer Engineering/Computer Architecture and Embedded Processors, ECE Department
- Faculty Committee, Integrated Circuits and Systems, ECE Department
- Graduate Studies Committee, ECE Department

8. Technical Society Service
Editorships, committee memberships, chairing sessions etc.

- Session Chair, Design Automation Conference (DAC)
- Organizer (with C. Haubelt), Special Session on "Embedded Multi-Processor Software Synthesis", Design Automation Conference (DAC)
- Registration Chair, International Symposium on Performance Analysis of Systems and Software (ISPASS)
- Chair, Technical Program Committee, Austin Conference on Integrated Circuits and Systems (ACISC)
- Co-organizer (with C. Haubelt), Workshop on Compiler-Assisted System-on-Chip Assembly (CASA)
- Member, Technical Program Committee, International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)
- Member, Technical Program Committee, Design, Automation and Test in Europe (DATE)
- Member, Technical Program Committee, International Conference on Computer Design (ICCD)
- Member, Technical Program Committee, International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)

D. Other Items of Interest

E. Plans for the Coming Year

- Resubmit NSF proposal on Linear Algebra Compute Fabrics (with R. van de Geijn)
- Resubmit SRC proposal on Heterogeneous Multicore Exploration (with L. John)
- Submit NSF CAREER proposal.
- Prepare and submit journal paper on Multi-Processor Software Compilation (with R. Doemer and G. Schirner)
- Prepare and submit journal versions of papers about Multicore Processor Modeling, Heterogeneous Multiprocessor SDF Mapping (with B. Evans), Linear Algebra Processor Design (with R. van de Geijn) and Video Transmission over Wireless Networks (with S. Vishwanath)
- Prepare and submit conference publications on research in Linear Algeba Processor Design, RTOS Modeling, Stochastic Simulation System-on-Chip Design, and System-Level Power Modeling.

SUMMARY OF ACTIVITIES FOR
Andreas Gerstlauer
September 1, 2011 – August 31, 2012

Research:

1. Awards and Honors

N/A

2. Invited Addresses and Colloquia

- "Teaching Experience: Developing a Class on Embedded Systems," in Young Faculty Workshop, Design Automation Conference (DAC), San Francisco, June 2012.
- "Heterogeneous System Design," Intel Research, Hillsboro, Oregon, March 2012.
- "A Low-Power, High-Performance Linear Algebra Core," NSF Center for Embedded Systems, Faculty of Computer Science and Engineering, Arizona State University, February 2012.
- "Software Synthesis for Embedded Multicore Systems," Keynote, Brazilian Symposium on Computing System Engineering (SBESC), Florianopolis, Brazil, November 2011.
- "A Low-Power, High-Performance Linear Algebra Core," Tech Topics Seminar Series, Advanced Micro Devices (AMD), Austin, TX, November 2011.
- "Circuit-Level Timing-Error Acceptance for Low Energy Signal Processing," Cirrus Logic, Austin, TX, November 2011.

3. Publications

(a) Journals and books
Indicate published, accepted for publication, revised or submitted and under review.

- K. He, A. Gerstlauer, M. Orshansky, "Circuit-Level Timing-Error Acceptance for Design of Energy-Efficient DCT/IDCT-based Systems," *IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)*, submitted, July 2012.
- D. Pfeifer, A. Gerstlauer, J. Valvano, "SimConnect and SimTalk for Distributed Cyber-Physical System Simulation," *Simulation: Transactions of the Society for Modeling and Simulation International*, revised, September 2012.
- J. Lin, B. Evans, A. Gerstlauer, "Communication-Aware Heterogeneous Multiprocessor Mapping for Real-Time Streaming Systems," *Journal of Signal Processing Systems*, vol. 69, no. 3, December 2012.
- A. Pedram, R. van de Geijn, A. Gerstlauer, "Co-Design Tradeoffs for High-Performance, Low-Power Linear Algebra Architectures," *IEEE Transactions on Computers (TC)*, special issue on Energy Efficient Computing, accepted for publication, May 2012.
- P. Razaghi, A. Gerstlauer, "Predictive OS Modeling for Host-Compiled Simulation of Periodic Real-Time Task Sets," *IEEE Embedded System Letters*, vol. 4, no. 1, March 2012.

(b) Refereed Conference Proceedings
Indicate published or accepted for publication.

- A. Pedram, A. Gerstlauer, R. van de Geijn, "On the Efficiency of Register File versus Broadcast Interconnect for Collective Communications in Data-Parallel Hardware Accelerators," *Proceedings of the IEEE/IFIP International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*, accepted for publication, August 2012.
- J. Massey, J. Starr, S. Lee, D. Lee, A. Gerstlauer, R. Heath, "Implementation of a Real-Time Wireless Interference Alignment Network," *Asilomar Conference on Signals, Systems and Computers*, accepted for publication, July 2012.
- D. Lee, H. Park, A. Gerstlauer, "Synthesis of Optimized Hardware Transactors from Abstract Communication Specifications," *Proceedings of the IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, accepted for publication, June 2012
- J. Miao, A. Gerstlauer, M. Orshansky, "Modeling and Synthesis of Quality-Energy Optimal Approximate Adders," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, accepted for publication, June 2012.
- A. Pedram, S. Z. Gilani, N. S. Kim, R. van de Geijn, M. Schulte, A. Gerstlauer, "A Linear Algebra Core Design for Efficient Level-3 BLAS," *Proceedings of the IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, Delft, The Netherlands, July 2012. (poster presentation)
- K. He, A. Gerstlauer, M. Orshansky, "Low-Energy Signal Processing using Circuit-Level Timing-Error Acceptance," Proceedings of the IEEE International Conference on Integrated Circuit Design and Technology (ICICDT), Austin, TX, May 2012. (invited paper)
- A. Gerstlauer, S. Chakravarty, M. Kathuria, P. Razaghi, "Abstract System-Level Models for Early Performance and Power Exploration," Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Sydney, Australia, January 2012. (invited paper)
- P. Razaghi, A. Gerstlauer, "Automatic Timing Granularity Adjustment for Host-Compiled Software Simulation," Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), Sydney, Australia, January 2012.
- D. Pfeifer, A. Gerstlauer, "Expression-Level Parallelism for Distributed Spice Circuit Simulation," *Proceedings of the IEEE/ACM International Symposium on Distributed and Real Time Applications (DS-RT)*, Manchester, United Kingdom, September 2011.
- M. S. Lopez, A. Gerstlauer, A. Avila, S. O. Martinez-Chapa, "A Programmable and Configurable Multi-port System-on-Chip for Stimulating Electrokinetically-Driven Microfluidic Devices," *Proceedings of the International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, Boston, MA, September 2011.
- A. Abdel-Hadi, J. Michel, A. Gerstlauer, S. Vishwanath, "Real-Time Optimization of Video Transmission in a Network of AAVs," *IEEE Vehicular Technology Conference (VTC)*, San Francisco, CA, September 2011.
- A. Pedram, A. Gerstlauer, R. van de Geijn, "A High-Performance, Low-Power Linear Algebra Core," *Proceedings of the IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, Santa Monica, CA, September 2011.

(c) Conference Presentations Without Proceedings of Full Papers

- A. Pedram, A. Gerstlauer, R. van de Geijn, "Overcoming Register File Inefficiencies by Using 2D Broadcast Bus Interconnects in Linear Algebra Accelerators," *3rd Workshop on SoCs, Heterogeneous Architectures and Workloads (SHAW-3)*, New Orleans, LA, February 2012.

3. Student Advising

(a) Completed PhD Theses

Names of students and program (e.g. ECE, CS, Physics, etc.)

- Ku He, "Adaptive Low-Energy Techniques in Memory and Digital Signal Processing Design," Electrical and Computer Engineering, University of Texas at Austin, April 18, 2012. (co-supervisor with Prof. Orshansky)
- Ahmed Abdel Hadi, "Multicast Networks: Capacity, Algorithms and Implementation," Electrical and Computer Engineering, University of Texas at Austin, October 17, 2011. (co-supervisor with Prof. Vishwanath)

(b) Current Graduate Advisees

PhD:

- Parisa Razaghi
- Hyungman Park
- Dongwook Lee
- Suhas Chakravarty
- Seogoo Lee
- Ardavan Pedram (with Robert van de Geijn, CS)
- Ku He (with Michael Orshansky)
- Jin Miao (with Michael Orshansky)
- Wei-Chen Su (part time)

MS:

- Ashmita Sinha
- Manan Kathuria

4. Current Research Projects and Grants

Title, agency, PI, role, amount, duration
Also list active research projects that are not funded (e.g. carried out by PhD level students)

- R. W. Heath (PI), A. Gerstlauer, "Interference Alignment in Distributed Environments," Army Research Office, $99,980, 8/2012-7/2013.
- A. Gerstlauer (PI), Lizy John, "Multi-dimensional Modeling, Design and Exploration of Heterogeneous Multicore SoCs," Contract 2012-HJ-2317, $345,000, 8/2012 – 7/2015
- A. Gerstlauer (PI), R. van de Geijn, "SHF:Small:Algorithm/Architecture Co-Design of Low Power and High Performance Linear Algebra Compute Fabrics," Grant CCF-1218483, $499,919, 6/2012 - 5//2015
- K. Pingali, A. Gerstlauer (co-PI), "Adaptive Hardware/Software Platforms for Mobile Web Browsing," Unrestricted, no-overhead gift, Qualcomm, BARD, Santa Clara, $80,000, 1/2012-12/2012.

- A. Gerstlauer (PI), "Automated Design Space Exploration and Optimization of DSP Systems," Unrestricted, no-overhead gift, National Instruments, Austin, $40,000, 8/2011-5/2012.
- A. Gerstlauer (PI), M. Orshansky, "Formal Synthesis of Low-Energy Signal Processing Systems Relying on Controlled Timing-Error Acceptance," National Science Foundation (NSF), Grant CCF-1018075, $449,676, 9/2010-8/2013.
- A. Gerstlauer (PI), "Automatic Platform Model Calibration and Tuning," Semiconductor Research Corporation (SRC), Contract 2010-HJ-2085, $255,000, 8/2010-7/2013.
- A. Gerstlauer, "Host-Compiled Multi-Core Software Simulation"

5. Proposal Submissions

Title, agency, PI, role, amount, duration

- A. Gerstlauer (PI), "CAREER: Network-Level Modeling and Design of Cyber-Physical Networks-of-Systems," $400,000, 09/2013 - 8/2018.
- L. John (PI), A. Gerstlauer, V. J. Reddi, R. van de Geijn, V. Eijkhout, L. Demkowicz, O. Ghattas, G. Biros, T. Wenisch (Univ. of Michigan, Ann Arbor), K. Fidkowski (Univ. of Michigan, Ann Arbor), "Co-Design of a Heterogeneous Hardware/Software Fabric for High-Performance Computational Fluid Dynamics," Air Force Office of Scientific Research, $5,919,077, 01/2013-12//2018.
- A. Gerstlauer (PI), H. Vikalo, "ABI Innovation: Stochastic In-Silico Simulation System for Genetic Regulatory Network Modeling and Inference," National Science Foundation, $489,592, 1/2012-12/2014

Teaching

6. Special Projects, Lab and Course Developments, etc.

Mentor, Senior Design Project, "MRI Simulation," 8/2011-5/2012.

C. Service Activities

7. University Service
Departmental and university-wide committees etc.

- Prospective Graduate Student Site Visit Coordinator, Integrated Circuits and Systems (ICS) track, ECE Department, UT Austin
- Graduate Admissions Committee, Computer Engineering/Computer Architecture and Embedded Processors, ECE Department
- Graduate Admissions Committee, Integrated Circuits and Systems, ECE Department
- Curriculum Committee, Computer Engineering/Computer Architecture and Embedded Processors, ECE Department
- Curriculum Committee, Integrated Circuits and Systems, ECE Department
- Faculty Committee, Computer Engineering/Computer Architecture and Embedded Processors, ECE Department
- Faculty Committee, Integrated Circuits and Systems, ECE Department
- Graduate Studies Committee, ECE Department

8. Technical Society Service

Editorships, committee memberships, chairing sessions etc.

- Topic Co-Chair (with P. Brisk), "Logic and high-level synthesis, SW synthesis, HW-SW co-design", International Conference on Very Large Scale Integration (VLSI-SoC)
- Subcommittee Chair, "EDA1: System-Level Design and Codesign", 2012 Design Automation Conference (DAC)
- Associate Editor, Design Automation for Embedded Systems (DAES)
- Member, Technical Program Committee, Design Automation Conference (DAC)
- Member, Technical Program Committee, International Conference on Very Large Scale Integration (VLSI-SoC)
- Member, Technical Program Committee, International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)
- Member, Technical Program Committee, Design, Automation and Test in Europe (DATE)
- Member, Technical Program Committee, International Conference on Computer Design (ICCD)
- Member, Technical Program Committee, Electronic System Level Synthesis Conference (ESLsyn)

D. Other Items of Interest

E. Plans for the Coming Year

- Resubmit NSF proposal on Stochastic Simulation System on Chip (with H. Vikalo)
- Submit NSF proposal on High-Level Synthesis for Reliability and Fault Tolerance.
- Prepare and submit journal paper on Multi-Processor Software Compilation (with R. Doemer, UC Irvine and G. Schirner, Northeastern Univ.)
- Prepare and submit journal version of RTOS & Processor Modeling research.
- Prepare and submit journal version of Hardware Transactor Synthesis research.
- Prepare and submit conference publications on research in Approximate Computing, Linear Algeba Processor Design, RTOS Modeling, Stochastic Simulation System-on-Chip Design, and System-Level Power Modeling.

SUMMARY OF ACTIVITIES FOR
ANDREAS GERSTLAUER
September 1, 2012 – August 31, 2013

A. Research:

1. Awards and Honors

- IEEE Computer Society Technical Committee on Parallel Processing (TCPP), Best Poster Award for student Ardavan Pedram at the Ph.D. Forum of the 2013 International Parallel & Distributed Processing Symposium (IPDPS)
- AMD Chair in Computer Engineering

2. Invited Addresses and Colloquia

- "System-Level Design of Embedded Systems," Department of Electrical Engineering and Information Technology, Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany, June 2013.
- "Models and Architectures for Heterogeneous System Design," Department of Computer Science, University of California, Los Angeles, Los Angeles, CA, May 2013.
- "Host-Compiled System Models for Early Power and Performance Exploration," Qualcomm Technologies (QCT), Inc., San Diego, CA, May 2013.
- "Models and Architectures for Heterogeneous System Design," Department of Computer Science and Engineering, University of California, San Diego, San Diego, CA, May 2013.
- "Models and Architectures for Heterogeneous System Design," Center for Embedded Computer Systems (CECS), University of California, Irvine, Irvine, CA, May 2013.
- "Models and Architectures for Heterogeneous System Design," Center for Experimental Research in Computer Systems (CERCS), Georgia Institute of Technology, Atlanta, GA, April 2013.
- "Models and Architectures for Heterogeneous System Design," Design of Robotics and Embedded Systems, Analysis and Modeling Seminar (DREAMS), Center for Electronic System Design/Center for Hybrid and Embedded Software Systems (CHESS), University of California, Berkeley, Berkeley, CA, April 2013.
- "Models and Architectures for Heterogeneous System Design," Center for Silicon System Implementation (CSSI), Carnegie Mellon University, Pittsburgh, PA, April 2013.
- "Dataparallel Accelerator Design beyond GPUs," IEEE CTS CAS/SSC/CEDA Workshop on Data Parallelism for Multi-Core Chips and GPU, Austin, TX, October 2012.

3. Publications

(a) Journals and books

Indicate published, accepted for publication, revised or submitted and under review.

- D. Pfeifer, J. Valvano, A. Gerstlauer, "SimConnect and SimTalk for Distributed Cyber-Physical System Simulation," *Simulation: Transactions of the Society for Modeling and Simulation International*, accepted for publication, November 2012.

- K. He, A. Gerstlauer, M. Orshansky, "Circuit-Level Timing-Error Acceptance for Design of Energy-Efficient DCT/IDCT-based Systems," *IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)*, vol. 3, no. 6, pp. 961-974, June 2013.
- J. Lin, A. Gerstlauer, B. L. Evans, "Communication-Aware Heterogeneous Multiprocessor Mapping for Real-Time Streaming Systems," *Journal of Signal Processing Systems*, vol. 69, no. 3, pp. 279-291, December 2012.
- A. Pedram, R. A. van de Geijn, A. Gerstlauer, "Codesign Tradeoffs for High-Performance, Low-Power Linear Algebra Architectures," *IEEE Transactions on Computers (TC)*, special issue on Energy Efficient Computing, vol. 61, no. 12, pp. 1724-1736, December 2012. (18% acceptance rate)

(b) Refereed Conference Proceedings
Indicate published or accepted for publication.

- J. Miao, A. Gerstlauer, M. Orshansky, "Approximate Logic Synthesis under General Error Magnitude and Frequency Constraints," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, November 2013. (26% acceptance rate)
- S. Lee, A. Gerstlauer, "Fine Grain Word Length Optimization for Dynamic Precision Scaling in DSP Systems," *Proceedings of the IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Istanbul, Turkey, November 2013. (20% acceptance rate, 28% incl. short papers)
- S. Chakravarty, Z. Zhao, A. Gerstlauer, "Automated, Retargetable Back-Annotation for Host Compiled Performance and Power Modeling," *Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Montreal, Canada, October 2013. (28% acceptance rate)
- A. Mariano, D. Lee, A. Gerstlauer, D. Chiou, "Hardware and Software Implementations of Prim's Algorithm for Efficient Minimum Spanning Tree Computation," *Proceedings of the International Embedded Systems Symposium (IESS)*, Paderborn, Germany, June 2013.
- H. Park, A. Gerstlauer, "Toward a Fast Stochastic Simulation Processor for Biochemical Reaction Networks," *Proceedings of the IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, Washington, DC, June 2013. (22% acceptance rate, 36% incl. short papers)
- A. Pedram, J. McCalpin, A. Gerstlauer, "Transforming A Linear Algebra Core to An FFT Accelerator," *Proceedings of the IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, Washington, DC, June 2013. (22% acceptance rate, 36% incl. short papers)
- P. Razaghi, A. Gerstlauer, "Multi-Core Cache Hierarchy Modeling for Host-Compiled Performance Simulation," *Proceedings of the Electronic System Level Synthesis Conference (ESLSyn)*, Austin, TX, June 2013. (38% acceptance rate)
- D. Pfeifer, A. Gerstlauer, J. Valvano, "Dynamic Resolution in Distributed Cyber-Physical System Simulation," *Proceedings of the ACM SIGSIM Conference on Principles of Advanced Discrete Simulation (PADS)*, Montreal, Canada, May 2013. (39% acceptance rate)
- A. Pedram, A. Gerstlauer, R. A. van de Geijn, "Floating Point Architecture Extensions for Optimized Matrix Factorization," *Proceedings of the 21st IEEE International Symposium on Computer Arithmetic (ARITH21)*, Austin, TX, April 2013. (28% acceptance rate)
- K. He, A. Gerstlauer, M. Orshansky, "Low-Energy Digital Filter Design Based on Controlled Timing Error Acceptance," *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, San Jose, CA, March 2013.
- J. Miao, K. He, A. Gerstlauer, M. Orshansky, "Modeling and Synthesis of Quality-Energy Optimal Approximate Adders," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, November 2012. (24% acceptance rate)

- J. W. Massey, J. Starr, S. Lee, D. Lee, A. Gerstlauer, R. W. Heath, "Implementation of a Real-Time Wireless Interference Alignment Network," *Proceedings of the Asilomar Conference on Signals, Systems and Computers (ACSSC)*, Pacific Grove, CA, November 2012. (invited paper)
- D. Lee, H. Park, A. Gerstlauer, "Synthesis of Optimized Hardware Transactors from Abstract Communication Specifications," *Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Tampere, Finland, October 2012. (28% acceptance rate)
- A. Pedram, A. Gerstlauer, R. A. van de Geijn, "On the Efficiency of Register File versus Broadcast Interconnect for Collective Communications in Data-Parallel Hardware Accelerators," *Proceedings of the IEEE International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*, New York, NY, October 2012. (28% acceptance rate)

(c) Conference Presentations Without Proceedings of Full Papers

None

3. Student Advising

(a) Completed PhD Theses

Names of students and program (e.g. ECE, CS, Physics, etc.)

- Ardavan Pedram, "Algorithm/Architecture Codesign of Low Power and High Performance Linear Algebra Compute Fabrics," Electrical and Computer Engineering, The University of Texas at Austin, July 29, 2013. (co-supervisor with Prof. van de Geijn, Computer Science)

(b) Current Graduate Advisees

PhD:

- Suhas Chakravarty (part time)
- Dongwook Lee
- Seogoo Lee
- Jin Miao (with Michael Orshansky)
- Hyungman Park
- Dylan Pfeifer (part-time, with Jonathan Valvano)
- Parisa Razaghi
- Wei-Chen Su (part time)

MS:

- Wenxiao Yu
- Zhuoran Zhao

4. Current Research Projects and Grants

Title, agency, PI, role, amount, duration

Also list active research projects that are not funded (e.g. carried out by PhD level students)

- A. Gerstlauer (PI), "Core Technology Development for System Simulation including Network," Sponsored Research Agreement UTA12-001141, Samsung Electronics, DMC R&D Center, Korea, $149,020, 6/2013-12/2013.
- A. Gerstlauer (PI), "Automated Design Space Exploration and Optimization of DSP Systems," Sponsored Research Agreement UTA12-000636, National Instruments, Austin, $60,000, 8/2012-7/2013.

- R. W. Heath (PI), A. Gerstlauer, "Interference Alignment in Distributed Environments," Army Research Office, $99,980, 8/2012-7/2013.
- A. Gerstlauer (PI), L. K. John, "Multi-dimensional Modeling, Design and Exploration of Heterogeneous Multicore SoCs," Semiconductor Research Corporation (SRC), Contract 2012-HJ-2317, $345,000, 8/2012 – 7/2015.
- A. Gerstlauer (PI), R. van de Geijn, "SHF:Small:Algorithm/Architecture Co-Design of Low Power and High Performance Linear Algebra Compute Fabrics," National Science Foundation (NSF), Grant CCF-1218483, $499,919, 6/2012 - 5//2015.
- A. Gerstlauer (PI), M. Orshansky, "Formal Synthesis of Low-Energy Signal Processing Systems Relying on Controlled Timing-Error Acceptance," National Science Foundation (NSF), Grant CCF-1018075, $449,676, 9/2010-8/2013, no-cost extension until 8/2014.
- A. Gerstlauer (PI), "Automatic Platform Model Calibration and Tuning," Semiconductor Research Corporation (SRC), Contract 2010-HJ-2085, $255,000, 8/2010-7/2013, no-cost extension until 8/2014.

5. Proposal Submissions

Title, agency, PI, role, amount, duration

- A. Gerstlauer (PI), "CAREER: Formal Models and Abstractions for Network-Level Design of Embedded Networks-of-Systems," National Science Foundation, $400,209, 9/2014 – 8/2019.
- G. Biros (PI), A. Gerstlauer, L. K. John, R. van de Geijn, "XPS: DSD: A2MA: Architectures and Algorithms for Multiresolution Scientific Applications," National Science Foundation, $749,801, 9/2013 - 8/2016
- V. Eijkhout (PI), J. McCalpin, A. Gerstlauer, "XPS: CLCCA: Explicit Hardware and Software Semantics for Data Movement in Parallel Computing," National Science Foundation, $749,935, 9/2013 - 8/2016.
- L. K. John (PI), A. Gerstlauer, "Adaptive Low Power Computing with Multiple Cores and Accelerators," Samsung Global Research Outreach (GRO), $299,973, 9/2013 – 12/2016
- A. Gerstlauer (PI), J. Valvano, "CPS:Breakthrough: Distributed, Parallel and Adaptive Coordination Backplanes for Large-Scale Cyber-Physical System Simulation," National Science Foundation, $496,241, 9/2013-8/1016
- A. Gerstlauer (PI), H. Vikalo, X. Cai (Univ. of Miami), "SHF:Small:Collaborative Research: Algorithms and Architectures for In-Silico Stochastic Simulation and Inference of Complex Genetic Networks," National Science Foundation, $424,766, 9/2013 - 8/2016

B. <u>Teaching</u>

6. Special Projects, Lab and Course Developments, etc.

- J. Valvano, R. Yerraballi, A. Gerstlauer, W. Bard, M. Erez, N. Telang, "Introduction to Embedded Systems (EE319K)," develop a pilot offering of a massively online open course (MOOC) as part of UTx, UT System's partnership with edX (non-profit provider of online courses founded by Harvard and MIT), course to launch in Spring 2014, course material will be test driven in the regular program in Fall 2013.

C. Service Activities

7. University Service

Departmental and university-wide committees etc.

- Prospective Graduate Student Site Visit Coordinator, Integrated Circuits and Systems (ICS) track, ECE Department, UT Austin
- Graduate Admissions Committee, Computer Engineering/Computer Architecture and Embedded Processors, ECE Department
- Graduate Admissions Committee, Integrated Circuits and Systems, ECE Department
- Curriculum Committee, Computer Engineering/Computer Architecture and Embedded Processors, ECE Department
- Curriculum Committee, Integrated Circuits and Systems, ECE Department
- Faculty Committee, Computer Engineering/Computer Architecture and Embedded Processors, ECE Department
- Faculty Committee, Integrated Circuits and Systems, ECE Department
- Graduate Studies Committee, ECE Department

8. Technical Society Service

Editorships, committee memberships, chairing sessions etc.

- Technical Area Chair, "Architecture and Implementation", 2013 Asilomar Conference on Systems, Signals and Computers
- Technical Program Co-Chair, 2013 Electronic System Level Synthesis Conference (ESLsyn)
- Track Co-Chair, "T8: Embedded Systems/HW-SW Codesign/Logic & High Level Synthesis", 2013 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)
- Subcommittee Chair, "EDA1: System-Level Design and Codesign", 2013 ACM/EDAC/IEEE Design Automation Conference (DAC)
- Associate Editor, ACM Transactions on Embedded Computer Systems (TECS)
- Associate Editor, Springer Design Automation for Embedded Systems (DAES)
- Member, Technical Program Committee, ACM/EDAC/IEEE Design Automation Conference (DAC)
- Member, Technical Program Committee, IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)
- Member, Technical Program Committee, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)
- Member, Technical Program Committee, Design, Automation and Test in Europe (DATE)
- Member, Technical Program Committee, IEEE International Conference on Computer Design (ICCD)
- Member, Technical Program Committee, Electronic System Level Synthesis Conference (ESLsyn)
- Member, Technical Program Committee, IFIP International Embedded Systems Symposium (IESS)
- Panel Reviewer, National Science Foundation

D. Other Items of Interest

E. Plans for the Coming Year

- Develop and teach MOOC offering of EE319K.
- Revamp EE382V graduate class (laboratory component) on System-on-Chip (SoC) Design.
- Graduate Ph.D. students Parisa Razaghi and Jin Miao.
- Prepare and submit journal and conference publications.

Budget Council Assessment of Teaching Performance for Faculty Promotion Candidate Andreas Gerstlauer

This report was prepared by Budget Council Members Professors Jonathan Valvano and Yale Patt, and is their personal evaluation of Professor Andreas Gerstlauer's teaching record.

Principal Areas of Teaching

Dr. Gerstlauer's principal area of research and teaching is in system level design of embedded systems. This involves the holistic design of both hardware and software to solve a domain specific computer problem, and requires applying engineering tradeoffs in accomplishing this goal. To that end, he teaches both graduate and undergraduate courses. He has focused his undergraduate teaching on EE319K, a core freshman course on hardware/software interfacing, which includes both software development and system integration of hardware and software components. At the graduate level, he has focused his attention on two courses, a new graduate course in "Embedded System Design and Modeling," (ESDM) which he developed and introduced at UT, and an existing lab-based course, "System on a Chip," (SoC) which he took over and overhauled. EE319K is required of all freshman majors in electrical and computer engineering. It is the first course wherein the student is faced with writing programs that interface the hardware and the software of an embedded system. The two graduate courses are fundamental for students wishing to either pursue a PhD in embedded systems architecture or assume leadership positions on design teams in industry.

Teaching Evaluation Procedures and Measures

The ECE department employs two teaching evaluation procedures: Course Instructor Surveys and peer evaluation. The course instructor surveys are conducted in the last three weeks of the semester in every course. A peer evaluation is made by a professor after a visit to the classroom. The time and date of the visit are agreed to beforehand so that the visit does not catch the instructor by surprise.

Summary of Course Instructor Surveys

The primary indicator on the Course Instructor Surveys used to evaluate teaching performance is the Overall Instructor Rating. Dr. Gerstlauer's evaluations are shown in the table below.

Class	Level	Semester	Enrollment	Instr. Rating*	Course Rating
EE319K	Undergraduate (freshmen, required)	Spring '09	38	4.1	4.2
		Spring '11	84	3.7†	3.3†
		Spring '12	73	4.3	3.7
		Spring '13	71	4.1	3.9
EE382V ESDM	Graduate (introductory)	Fall '08	19	4.4	3.8
		Fall '09	26	3.8	3.5
		Fall '10	15	4.1	3.9
		Fall '11	14	4.5	3.9
EE382V SoC	Graduate (introductory)	Spring '10	18	4.6	4.3
		Spring '11	10	4.2	3.6
		Fall '12	41	4.2	3.7

* Average/median/standard deviation of instructor ratings for ECE tenured/tenure-track faculty is 4.06 / 4.08 / 0.42 for undergraduate courses, 4.22 / 4.36 / 0.37 for graduate courses, and 4.12 / 4.04 / 0.29 for EE319K.
† An electronic course evaluation was performed, but only 26 responses were collected.

The table lumps his teaching performance into three sections, one section for each of the three courses he has taught.

It is clear that the students consider Dr. Gerstlauer an outstanding teacher. Of the eleven classes he has taught, nine of them are ranked at 4.1 or higher. Two classes were ranked below 4.0, the freshman course EE319K in Spring, 2011 (3.7), and the graduate Embedded Systems Design and Modeling course in Fall, 2009 (3.8). Given the overwhelming positive evaluations in all three courses, we see the two courses below 4.0 as outliers, and hence, we do not have reason for concern.

In fact, one of the outliers, the 3.7 evaluation for EE319K in Spring, 2011, can be explained easily. The course was evaluated electronically with only 30% of the students in the class participating in the evaluation. Normally, we use paper evaluations, and normally a much higher percentage of the students in each class participate.

Summary of Peer Evaluation

Dr. Gerstlauer's classes were evaluated by both of us, Professor Jonathan Valvano performing the peer evaluation in March, 2012, and Professor Yale Patt performing the peer evaluation in March, 2013. Both of us rank Dr. Gerstlauer as an outstanding teacher, citing his clear explanations, comfortable manner in the classroom, and his effective use of both the blackboard and technology in getting his points across. These evaluations are included in the promotion packet.

Comparison with other instructors in the ECE Department

EE319K is a very demanding, but critical, course required of all ECE majors during their freshman year. As such, the ECE department has assigned the course to instructors who are known for being conscientious and excellent teachers. Not surprising, even though the course requires a lot of effort from students, it is a popular freshman course and routinely receives positive evaluations.

Listed below are the CIS evaluations for the six instructors who have been teaching the course since 2009.

This is the most appropriate course to use as a metric to compare Professor Gerstlauer with his peers for two reasons: (1) it is the undergraduate course that he has focused on, and (2) the sample size is large enough (1744 students, 29 classes) to provide meaningful data.

His CIS instructor average numbers are right at the overall average of 4.1. His CIS course numbers are slightly below the overall average of 3.9. His class GPA is slightly lower than the overall average GPA of 3.07, suggesting there is no bias in evaluation scores caused by perceived grade expectations. This data places him right at the average among the excellent instructors teaching this course.

Gerstlauer		Professor 1		Professor 2	
CIS Instructor	4.1	CIS Instructor	3.9	CIS Instructor	3.7
CIS Course	3.8	CIS Course	3.9	CIS Course	3.8
GPA	3.03	GPA	3.13	GPA	3.00
Class Size	59	Class Size	41	Class Size	53
Professor 3		Professor 4		Professor 5	
CIS Instructor	4.1	CIS Instructor	4.2	CIS Instructor	4.5
CIS Course	3.9	CIS Course	4.0	CIS Course	4.0
GPA	3.19	GPA	3.04	GPA	3.05
Class Size	50	Class Size	68	Class Size	67

Table. CIS/GPA data since 2009 of all EE319K instructors (source. CIS, www.myedu.com). Professor Gerstlauer's data are highlighted.

Massively Open Online Course (MOOC)

The University of Texas at Austin will deliver nine online classes in the MOOC format during the 2013-2014 academic year. EE319K will be one of these pilot classes, with a scheduled launch in Spring 2014. Professor Gerstlauer is one of three faculty (along with Ramesh Yerraballi and Jonathan Valvano) involved in the design and delivery of this online class. In particular, his role to date has been overall course design, selection of topics for inclusion, and review of teaching materials. Professor Gerstlauer's role has been restricted over the summer as he focuses on his promotion package. During the fall semester leading up to the Spring 2014 launch he will take a more active role in design and creation of educational content.

Balance Between Graduate and Undergraduate Teaching

Dr. Gerstlauer's teaching load was two courses per year during his first two years on the ECE faculty (2008-09, 2009-10), three courses per year (2010-11, 2011-12), and two courses per year, starting in Fall, 2012. This is consistent with ECE's normal policy toward teaching loads, wherein new assistant professors were assigned two courses per year during their first two years on the faculty, and three courses per year for research active faculty after that. Starting in Fall, 2012, all research active faculty have been assigned two courses per year.

Dr. Gerstlauer has achieved a commendable balance between undergraduate and graduate teaching. He has taught the freshman course four times and his two graduate courses a total of seven times.

Individual Instruction

Dr. Gerstlauer has an excellent record in the area of individual instruction, and has gone out of his way to do more than his share when it comes to taking on responsibilities involving individual instruction.

Dr. Gerstlauer has been the co-advisor of three students who have completed their PhDs at UT. He has also been the co-advisor of two students who completed their PhDs elsewhere. He also served on the PhD dissertation committees of eight students who completed their PhDs at The University of Texas, and two students who completed their PhDs at universities in Germany. He is currently advising five PhD students at UT as the sole advisor, plus two additional PhD students as co-advisor.

Dr. Gerstlauer has also supervised 3 completed MS theses and 5 MS reports.
He is a member of the PhD dissertation committees of ten PhD students at UT. He is a member of the MS thesis committees of three MS students at UT, one MS student at UC Irvine, and three MS students at universities in Germany. He is a member of the MS Report committee of three MS students at UT.

The ECE department has a graduation requirement wherein every student must participate in a senior design project. Projects are done by four or five person teams and take two semesters to accomplish. The members of each team meet weekly throughout the two semesters with their faculty mentor. Dr. Gerstlauer has mentored two undergraduate senior design projects.

Teaching Portfolio

Dr. Gerstlauer has prepared an 8-page teaching philosophy statement which expresses in depth his attitude toward teaching and his views on what it takes to do effective teaching. He discusses how his views have evolved over the time he has been teaching.

Dr. Gerstlauer has also prepared a comprehensive portfolio of the teaching materials used in his three courses. They are included in this promotion packet.

Conclusion

In summary, while in rank as an Assistant Professor at UT Austin, Dr. Gerstlauer has delivered very high quality teaching at all student levels, both in formal classes and in supervision of individual work. He is well deserving of tenure and promotion to the rank of Associate Professor.

Respectfully,

Jonathan W. Valvano
Professor of Electrical and Computer Engineering, and
Engineering Foundation Centennial Teaching Fellow in Electrical Engineering #1

Yale N. Patt
Professor of Electrical and Computer Engineering,
Ernest Cockrell, Jr. Centennial Chair in Engineering, and
Distinguished University Teaching Professor

ANDREAS GERSTLAUER
Statement on Teaching

Teaching is the primary mission and the way in which we as academics and educators can have a lasting impact on future generations and hence society. Grounded in my research in computer engineering, my teaching philosophy as instructor in this area is based on bridging theoretical and practical aspects as well as motivating students by always providing the bigger context of material taught in class. Tight integration of research with teaching is thereby reinforced by the observation that effective teaching in addition to critical advising are reciprocally rewarding for both the teacher and the student. On the one hand, the teacher successfully communicates an often eye-opening new concept while on the other hand, the student can extend the current body of knowledge through novel interpretations. Overall, I believe that teaching should not solely be focused on a narrow band of scientific knowledge but should rather follow a comprehensive strategy that also considers practical and human aspects.

Throughout my time as a graduate student, post-doctoral researcher and professor, I have regularly been engaged in the teaching process, serving initially as a teaching assistant (TA) and later as instructor on record, thesis advisor and research project leader. In addition, I have communicated my research results in the form of numerous invited lectures or as part of industry or conference tutorials over the years. Since coming to UT Austin, I have been a regular instructor for one of our core required freshmen classes, I have developed and regularly taught two introductory graduate classes, and I have mentored and advised both undergraduate and graduate students on senior design projects and research.

TEACHING EXPERIENCE

My early teaching experience as an assistant and lecturer for undergraduate and graduate courses on computer networking and digital logic, computer, and embedded system design laid the early foundations for my continued interest and passion in imparting knowledge onto future generations of engineers and scientists. During my time as research professor at UC Irvine, I actively pursued, in addition to research, a position as lecturer in the Department of Electrical Engineering and Computer Science. In that capacity, I enjoyed being the instructor on record for a cross-listed introductory course on digital system design (EECS/CSE 31, "Introduction to Digital Systems") with more than 100 enrolled lower-division undergraduate students (instructor rating of 3.06 out of a 4-point scale).

In my current position as Assistant Professor at UT Austin, I regularly teach one undergraduate and two graduate classes. At the graduate level, I created and introduced a new introductory class EE382V, "Embedded System Design and Modeling," with a research-oriented focus on system-level modeling and design of embedded systems. In addition, I have taken over responsibilities for and significantly revamped an existing lab-based class EE382V, "System-on-a-Chip Design." Finally, at the undergraduate level, I am regularly teaching our core freshmen class on programming and hardware/software interfacing (EE319K, "Introduction to Embedded Systems"). I received excellent student evaluations for all classes taught, including praise from senior students for being one of the best teachers. A summary of my teaching activities and evaluations (on a 5-point scale) is provided in the following table:

Class	Level	Semester	Enrollment	Instr. Rating*	Course Rating
EE319K	Undergraduate (freshmen, required)	Spring '09	38	4.1	4.2
		Spring '11	84	3.7†	3.3†
		Spring '12	73	4.3	3.7
		Spring '13	71	4.1	3.9
EE382V ESDM	Graduate (introductory)	Fall '08	19	4.4	3.8
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* Average/median/standard deviation of instructor ratings for ECE tenured/tenure-track faculty is 4.06 / 4.08 / 0.42 for undergraduate courses, 4.22 / 4.36 / 0.37 for graduate courses, and 4.12 / 4.04 / 0.29 for EE319K.
† An electronic course evaluation was performed, but only 26 responses were collected.

In addition to classes, I have also enjoyed the opportunity to serve as a mentor and (co-) supervisor for undergraduate, masters and Ph.D. students. I have had undergraduate students involved in my lab and I have mentored two undergraduate senior design teams. At the graduate level, I have served on 10 Ph.D. defense committees of non-advised students (2 at universities in Germany), 23 Ph.D. candidacy exams (21 at UT Austin with 4 as supervisor), and as reader for 10 M.S. reports or theses. Under my supervision, I have graduated 4 full-time M.S. students, 3 part-time M.S. students, and 2 M.S. students (1 co-advised) continuing for their Ph.D. In addition, I have co-advised 5 students to completion of their Ph.D. dissertations (3 at UT Austin). My first solo-advised student is expected to graduate in Fall 2013.

Due to the interest my research has attracted, I have also been invited to lecture on numerous occasions in both academia and industry. I have given tutorials in industrial research labs and development groups at companies like Xilinx, Motorola, IBM, BMW and Bosch. Furthermore, I have been a speaker in several tutorials at high-profile international conferences. In all cases, tutorials were well received with audiences exceeding 50 attendees. For example, System-Level Specification Beyond RTL was the best attended tutorial at the Design, Automation and Test in Europe (DATE) conference in 2002.

TEACHING METHODOLOGY AND PHILOSOPHY

Overall, through my teaching and advising, one key insight that I came to realize is that the practical relevance of presented information is paramount to imparting knowledge, especially in the fields of computer science and engineering. Specifically, comparing my time as a student back in Germany with my experiences both as a student and teacher at UCI and UT Austin, I learned that following up theoretical classroom lectures with their practical application in homework or labs is beneficial and crucial for students to learn and retain, but most critically to extend the current knowledge in the long term. As such, all my classes have significant lab and homework components. Furthermore, in both my undergraduate and graduate classes, I provide a practical perspective through regular guest lectures by speakers from industry or by faculty in other areas. For graduate classes, I also replace the final exam with a class project that further exposes students to real-world research or industry problems.

I believe that teaching effectiveness depends to a large part on properly motivating students by teaching not only how things are done but also why. One has to strive to provide the big picture in context and the application of a certain concept being taught. I therefore always introduce a new topic in class with a discussion of its background and importance including why and where it fits into the overall theme of the class. Likewise, before switching to a new topic, I always first summarize the current one by relating it back to the larger story. This also provides me with an opportunity to engage students by querying them about their perspective on a specific problem (at the start of a new topic) and by formally or informally quizzing them on their understanding of key concepts in previously presented material within the larger context of the class (at the conclusion of a topic).

My lecture style has evolved over the years from solely relying on slides to settling on a mix of whiteboard notes, interactive examples and slides that summarize and frame the discussion. I have found this style to be very effective in keeping students interested, motivated and engaged. I use slides to introduce and summarize a problem area at the start or conclusion of each topic. By contrast, I develop the actual problem formulations and solutions in detail on the board. This setup allows me to combine the best of both worlds, i.e. the interactivity of the whiteboard with the comprehensiveness of slides. My slide sets include properly formatted copies of all whiteboard notes, and I aim to make all slides available to students as lecture notes well in advance of each class. This allows students to study the material and prepare before coming to lecture. Overall, it is my philosophy to freely distribute all my teaching materials, lecture notes and lab or homework exercises on the web. As detailed below, material that I developed for my graduate classes has been adopted by several faculty at universities worldwide for their own courses.

Another important component of my teaching is continuous feedback and improvement. Especially in fast-moving fields such as computer engineering, it is crucial to adapt and update course content with new developments out of research and industrial practice every time a class is taught. Furthermore, during each semester, I actively solicit feedback from students through 1 or 2 (anonymous) electronic mid-term surveys that allow me to tailor and fine tune content. In many cases, I have also used feedback from mid-term or final surveys to make significant changes in future offerings, such as adjusting my lecturing style or redistributing weight and content among homework and labs in my graduate classes. Finally, I strive to be always available for students even outside of class and regular office hours. I often hold extra office hours or review sessions, I visit undergraduate labs to see how students are doing, and I generally make myself available before and after each lecture to answer questions or provide support.

COURSE DEVELOPMENT

Graduate Classes When I first joined UT Austin in Fall 2008, I took the opportunity to create and introduce a new graduate class (EE382V, "Embedded System Design and Modeling") to fill a gap in the curriculum in my own research area. This class is developed around a recent textbook on embedded system design co-authored by myself together with former colleagues at UC Irvine [B7]. It is geared towards research topics with a focus on abstract, format concepts, techniques and methods for system-level design, which are complemented by lab exercises and homework using the System-on-Chip Environment (SCE) tool set developed in my group. As such, the class is designed to tightly integrate with my research. Lecture, lab and homework materials are continuously updated to integrate recent research results and thus expose students to novel concepts emerging both from my group and from other researchers in the area. At the same time, I have been very successful in letting feedback and new ideas from interactions with students flow back into my research. As their final class project, students can freely explore a research topic of their choosing, where I work closely with them on suggesting and picking rewarding topics and on advising them throughout their projects. As a result, around 10-20% of the projects have led to publications [C23, C24, C32, C34] and, in some cases, even advanced research projects for the students [J10]. Overall, the class provides a strong example of the benefits gained from integrating teaching with research. This is further exemplified by the fact that the class is often taken by students from areas other than Computer Engineering. Furthermore, the textbook and class materials developed by myself (such as lecture notes and exercises around the SCE tool set) have been adopted at several other universities worldwide, including Iowa State University, Northeastern University, Concordia University, Leiden University in the Netherlands, Istanbul Technical University, Turkey, the Federal University of Pernambuco, Brazil, the University of Teheran, Iran, and the Universities of Oldenburg and Stuttgart in Germany.

Since coming to UT Austin, I have also taken over responsibilities for an existing course on "System-on-Chip (SoC) Design" (EE382V) that was originally developed by my colleague Mark McDermott. This class focuses on state-of-the-art industrial practices with a significant lab component and final project in which students have to realize a SoC design of a software-defined/digital radio receiver on an ARM and FPGA based prototyping platform. Since taking over the class, I have adjusted the course content of both my graduate classes to complement each other, ensuring that they can be taken in a sequence of any order, i.e., either following a top-down or a bottom-up flow. All formal system-level design content from specifications to SoC architecture exploration has been concentrated in the previously described class. By contrast, the SoC class has been revamped to emphasize theory and practice of component-level hardware and software implementation starting from a given architecture. This is complemented by new lab exercises and a final project in which students use industry-standard tools such as Open Virtual Platform (OVP) for SystemC-based modeling, and Calypto (formerly Mentor) Catapult for high-level hardware synthesis. In doing so, I have interfaced with tool vendors to acquire corresponding licenses as well as generating associated lecture and lab content. I have taught this class both in our regular graduate program (a total of 3 times as summarized on page 1) as well as in a professional masters program for external students from industry (also 3 times). All combined, both of my graduate classes continue to be regularly taught and are continuously being updated to provide a state-of-the-art graduate-level education and an integrated lecture sequence on both frontend and backend embedded system/SoC design processes.

Undergraduate Classes At the undergraduate level, I have been actively involved in the teaching and development of the core computer engineering curriculum for the Electrical and Computer Engineering Department at UT Austin. Together with a team of other computer engineering faculty, I am regularly teaching an introductory class on microcontroller programming and hardware/software interfacing (EE319K), which is the first class in the undergraduate sequence on embedded systems at UT Austin. As an active member of the computer engineering curriculum committee, I participated in a curriculum reform that resulted in the decision to further strengthen the bottom-up philosophy in teaching computer engineering and embedded system concepts at UT. From our experience, this has proven to be a very effective approach, and our graduates are highly valued by local industry as some of the best programmers coming out of any department or school. As a result of the reform, we have been revamping EE319K and moving it into the Freshman year. In the process, we have also switched to an ARM architecture for the class' significant lab component, which lets students apply the concepts taught in class to the programming of microcontrollers and interfacing with real hardware. After an introduction to computers in their first semester, the revamped EE319K now exposes students to their first actual

programming experience, all in an embedded context. As part of the core EE319K teaching team, I have participated in the process of developing and upgrading lecture, lab and homework content to implement the new bottom-up strategy in which students are now taught basic programming concepts simultaneously in both assembly and C. This builds the foundation for later classes to expand on C (and later Java) programming as well as hardware (digital logic) design.

Looking forward, I am interested in further broadening my participation in undergraduate and general education. My plan is to take over teaching of our senior-level embedded class and introduce a hardware/software co-design component currently lacking in undergraduate curricula. Furthermore, with the UT System having recently joined the edX consortium, our EE319K class has been selected as one of the pilot offerings for a massively open online course (MOOC) under the UTx umbrella. I am part of the team developing the UTx EE319K course, which is expected to become one of the first MOOCs worldwide that integrates a significant lab component into a massive online learning experience. We are currently developing associated online video, lecture and lab content. In Fall 2013, I will be teaching EE319K in the regular program using a flipped classroom setting to test-drive the material in preparation for the official MOOC launch in Spring 2014. I am excited about the opportunity to explore one possible future of education, and I look forward to being part of the MOOC team going forward.

INDIVIDUAL INSTRUCTION

One of the most rewarding aspects as an educator are my personal interactions with graduate and undergraduate students to pass on my experiences and guide, advise and mentor them. Combined with experiences from presenting my research at conferences, invited talks or tutorials, regular interactions with students extending from inside to outside of the classroom are not only the key to effective mentoring and teaching, but are a necessary and crucial means to obtain feedback and to provide mutually beneficial inspiration for the advancement of one's own abilities and goals.

Already during my time as senior Ph.D. student and research faculty, I had the opportunity to serve as a co-advisor for several masters and Ph.D. students as well as the lead for a team of post-doctoral project scientists and staff members in a large external research project. At UT Austin, I am currently supervising or co-supervising 9 graduate students. I have graduated 4 full-time terminal M.S. students, all of whom have gone on to industry positions at well-respected companies, such as Intel or National Instruments. I have also supervised 3 M.S. projects and reports of part-time students from industry who subsequently graduated from our professional masters program (in which I also teach my SoC Design class). In addition, due to family reasons, one student who completed his M.S. (Suhas Chakravarty) has taken a position with Freescale back in India while continuing to work on his Ph.D. part-time with me.

Two students I co-advised, Ahmed Abdel Hadi and Ku He, have graduated with their Ph.D.s in 2011 and 2012 and have subsequently taken on a post-doctoral position at Virginia Tech and a position in industry at Cirrus Logic, respectively. Another co-supervised student, Ardavan Pedram, will defend his Ph.D. dissertation in July 2013. He recently won the IEEE Computer Society Technical Committee on Parallel Processing (TCPP) Best Poster Award at the 2013 IEEE International Parallel & Distributed Processing Symposium (IPDPS) Ph.D. forum for his work. Finally, my first solo-advised student, Parisa Razaghi, passed her qualifying exam in Spring 2012 and is expected to complete her Ph.D. in Fall 2013.

At the undergraduate level, I often have students who take my freshmen class express interest in participating in research in my group. As such, I had several of these students join my group, e.g. over the summer. In addition, I have mentored two senior design projects with 5 students each on projects performed in close collaboration with industry. In a project sponsored by Texas Instruments (TI), this involved mapping of MRI algorithms onto one of TI's newly released high-performance DSP platforms. In the other case, in a project sponsored by ARM, students successfully implemented a digital, wirelessly-enabled Post-It display using a combination of hardware and software on an ARM-based FPGA platform. In all cases, I immensely enjoy interactions with undergraduates, which have often led to long-term interactions that I hope to be able to maintain over the duration of their careers.

Overall, I aim to maintain an open and collaborative environment in my research group. While each student is different, I generally strive to encourage independent, creative and critical thinking, providing guidance if and whenever it is necessary, but not micro-managing each aspect. My goal is thereby for students to learn the power of effectively working in teams, where they work with each other as much as possible and, in the long run, establish a hierarchy in which senior students can help advise the junior ones. Crucially, this is facilitated by establishing research projects in which multiple students can work on separate aspects yet learn from each other towards achieving a larger common goal.

SUMMARY OF TEACHING ACTIVITIES

Teaching Statistics

	2008-2013			Last 3 Years		
Metric	Total	Undergrad	Graduate	Total	Undergrad	Graduate
Students Taught	409	266	143	294	214	80
Avg. Weighted GPA	3.27	3.04	3.66	3.23	3.05	3.70
Avg. Instructor Rating	4.16	4.10	4.23	4.15	4.11	4.24
Avg. Course Rating	3.77	3.74	3.79	3.71	3.67	3.76

Course Schedule by Semester in ECE since 2008 (number of students indicated)

Course	F'08	S'09	F'09	S'10	F'10	S'11	F'11	S'12	F'12	S'13
EE319K		38				84		73		71
EE382V.ESDM	19		26		15		14			
EE382V.SoC				18		10			41	

Student Supervision

Student Type	In Rank (As Sole Advisor)	Total (As Sole Advisor)
Ph.D. Graduated*	1.5 (0)	2.5 (0)
Ph.D. In Candidacy*	2 (1)	
Ph.D. In Progress*	4 (4)	
M.S. Graduated*	7.5 (7)	7.5 (7)
M.S. In Progress*	2 (2)	

* Counted as 1 if sole advisor, 0.5 if co-advised

Current Graduate Students Supervised at UT Austin

Student	Co-Supervisor	Degree	Start	Expected
Dylan Pfeifer (part-time)	Jonathan Valvano	Ph.D.*	09/2008	Fall 2013
Parisa Razaghi	-	Ph.D.*	09/2009	Fall 2013
Jin Miao	Michael Orshansky	Ph.D.*	09/2010	Fall 2014
Hyungman Park	-	Ph.D.	09/2009	Spring 2015
Suhas Chakravarty (part-time)	-	Ph.D.	09/2009	Fall 2015
Dongwook Lee	-	Ph.D.	09/2009	Spring 2015
Seogoo Lee	-	Ph.D.	09/2011	Fall 2016
Wenxiao Yu	-	M.S./Ph.D.	09/2012	Fall 2014/2017
Zhuoran Zhao	-	M.S./Ph.D.	09/2012	Fall 2014/2017

* In candidacy

LIST OF STUDENT SUPERVISIONS

Postdoctoral Fellows Supervised

None

Ph.D. Dissertations Supervised

5. Ardavan Pedram, "Algorithm/Architecture Codesign of Low Power and High Performance Linear Algebra Compute Fabrics," Electrical and Computer Engineering, The University of Texas at Austin, July 29, 2013. (co-supervisor with Prof. van de Geijn, Computer Science)
4. Ku He, "Adaptive Low-Energy Techniques in Memory and Digital Signal Processing Design," Electrical and Computer Engineering, The University of Texas at Austin, April 18, 2012. (co-supervisor with Prof. Orshansky)
3. Ahmed Abdel Hadi, "Multicast Networks: Capacity, Algorithms and Implementation," Electrical and Computer Engineering, The University of Texas at Austin, October 17, 2011. (co-supervisor with Prof. Vishwanath)
2. Martha Salome Lopez De La Fuente, "Definition, Design and Implementation of a Processor-Based Stimulation System for Electrokinetically-Driven Fluidic Devices," Information Technologies and Communications, Monterey Institute of Technology, Monterey, Mexico, May 11, 2011. (external co-advisor with Prof. Sergio O. Martinez Chapa)
1. Gunar Schirner, "Improving Accuracy of Transaction Level Models in System-on-Chip Design," Electrical Engineering and Computer Science, University of California, Irvine, March 3, 2008. (co-advisor with Prof. Dömer)

M.S. Thesis Supervised

8. Jin Miao, "Modeling and Synthesis of Quality-Energy Optimal Approximate Adders," Electrical and Computer Engineering, The University of Texas at Austin, December 2012. (co-supervisor with Prof. Orshansky)
7. Ashmita Sinha, "Multi-Objective Trade-Off Exploration for Cyclo-Static and Synchronous Dataflow Graphs," Electrical and Computer Engineering, The University of Texas at Austin, August 2012.
6. Arindam Goswami, "ExtractCFG: A Framework to Enable Accurate Timing Back Annotation of C Language Source Code," Electrical and Computer Engineering, The University of Texas at Austin, August 2011.

M.S. Reports Supervised

5. Manan Kathuria, "A Framework for Automation of System-level Design Space Exploration," Electrical and Computer Engineering, The University of Texas at Austin, May 2012.
4. John Patrick Tourish, "dspIP: A TCP/IP Implementation for a Digital Signal Processor," Master of Science in Engineering, The University of Texas at Austin, May 2011.
3. Pablo Salinas Bomfim, "Integration of Virtual Platform Models into a System-Level Design Framework," Electrical and Computer Engineering, The University of Texas at Austin, May 2010.
2. Joel Williams, "Prototyping of MP3 Decoding and Playback on an ARM-based FPGA Development Board," Master of Science in Engineering, The University of Texas at Austin, May 2010.
1. Peter James Overholt, "Desktop Simulation of a Digital Signal Processing Design Flow using Synchronous Dataflow Modeling," Master of Science in Engineering, The University of Texas at Austin, August 2009.

Ph.D. Dissertation Committee Member

10. Muhammad Faisal Iqbal, "Workload-Aware Network Processors: Improving Performance While Minimizing Power Consumption," Electrical and Computer Engineering, The University of Texas at Austin, July 16, 2013.
9. Muhammad Tauseef Rab, "Techniques To Minimize Circuitry and Improve Efficiency for Defect Tolerance," Electrical and Computer Engineering, The University of Texas at Austin, April 18, 2013.
8. Jongwook Sohn, "Improved Architectures for Fused Floating-Point Arithmetic Units," Electrical and Computer Engineering, The University of Texas at Austin, March 22, 2013.
7. Evgeni Krimer, "Improving Energy Efficiency of Reliable Massively-Parallel Architectures," Electrical and Computer Engineering, The University of Texas at Austin, April 30, 2012.

6. Alexander Viehl, "Quantitative Synchronisationsanalyse kommunizierender Prozesse zum Echtzeitnachweis verteilter eingebetteter Systeme," Faculty of Science, University of Tubingen, Germany, January 9, 2012.
5. Rudrajit Dutta, "Adaptable and Enhanced Error Correction Codes for Efficient Error and Defect Tolerance in Memories," Electrical and Computer Engineering, The University of Texas at Austin, November 21, 2011.
4. Wooyoung Jang, "Architecture and Physical Design for Advanced Networks-on-Chip," Electrical and Computer Engineering, The University of Texas at Austin, April 25, 2011.
3. Sriram Sambamurthy, "Power Estimation of Microprocessors," Electrical and Computer Engineering, The University of Texas at Austin, May 19, 2010.
2. Henning Zabel, "Techniken zur Simulation von eingebetteten Systemen mit abstrakten RTOS-Modellen," Electrical Engineering, Computer Science and Mathematics, University of Paderborn, Germany, March 19, 2010.
1. Shayak Banerjee, "Enhancing the Design-Manufacturing Interface in Nanoscale Technologies," Electrical and Computer Engineering, The University of Texas at Austin, May 3, 2010.

Ph.D. Qualifying Examination Committee Member

23. Minsoo Rhu, "Performance-Efficient Mechanisms for Managing Irregularity in Throughput Processors," Electrical and Computer Engineering, The University of Texas at Austin, August 19, 2013. (chair)
22. Gene Wu, "Automated Abstract Power and Confidence Model Generation," Electrical and Computer Engineering, The University of Texas at Austin, May 2, 2013.
21. Jin Miao, "Design and Synthesis of Approximate Digital Circuits," Electrical and Computer Engineering, The University of Texas at Austin, May 1, 2013. (co-supervisor)
20. Ameya Chaudhari, "Ensuring Software Security and Processor Reliability using Runtime Processor Execution Monitoring," Electrical and Computer Engineering, The University of Texas at Austin, February 6, 2013.
19. Mahesh Prabhu, "Application of Formal Methods to Post-silicon Test and Debug," Electrical and Computer Engineering, The University of Texas at Austin, December 17, 2012.
18. Nicholas Paine, "High Performance Series Elastic Actuation," Electrical and Computer Engineering, The University of Texas at Austin, December 6, 2012.
17. Muhammad Faisal Iqbal, "Efficient System Level Power Management in Communications Processors," Electrical and Computer Engineering, The University of Texas at Austin, October 15, 2012.
16. Parisa Razaghi, "A Host-Compiled Multi-Core Software Simulation Platform," Electrical and Computer Engineering, The University of Texas at Austin, April 4, 2012. (supervisor)
15. Jungwook Sohn, "Improved Architectures for Floating-Point Fused Arithmetic Units," Electrical and Computer Engineering, The University of Texas at Austin, April 4, 2012.
14. Tauseef Raab, "Techniques to Minimize Circuitry and Improve Efficiency for Defect Tolerance," Electrical and Computer Engineering, The University of Texas at Austin, March 7, 2012.
13. Hari Angepat, "Accelerating Multicore System Design Through Functional Timing Decomposition," Electrical and Computer Engineering, The University of Texas at Austin, October 7, 2011.
12. Dylan Pfeifer, "Heterogeneous, Multi-Domain, Mixed Signal Hardware/Software Co-simulation," Electrical and Computer Engineering, The University of Texas at Austin, June 30, 2011. (co-supervisor)
11. Ku He, "Adaptive Low-Energy Techniques in Memory and Digital Signal Processing Design," Electrical and Computer Engineering, The University of Texas at Austin, April 29, 2011. (co-supervisor)
10. Ardavan Pedram, "Algorithm-Architecture Co-Design of a High Performance, Low Power Linear Algebra Processor," Electrical and Computer Engineering, The University of Texas at Austin, April 27, 2011. (co-supervisor)

9. Evgeni Krimer, "Improving Energy Efficiency of Massively Parallel Architectures," Electrical and Computer Engineering, The University of Texas at Austin, April 15, 2011.
8. Nikhil Patel, "Enforcing Architectural Contracts in High-Level Synthesis," Electrical and Computer Engineering, The University of Texas at Austin, March 7, 2011.
7. Ahmed Abdel Hadi, "Multicast Networks: Capacity, Algorithms and Implementation," Electrical and Computer Engineering, The University of Texas at Austin, August 23, 2010. (co-supervisor)
6. Rudrajit Dutta, "Enhancing Memory ECC through Post-Silicon Optimization," Electrical and Computer Engineering, The University of Texas at Austin, May 13, 2010.
5. Wooyoung Jang, "Architecture and Physical Design for Advanced Networks-on-Chip," Electrical and Computer Engineering, The University of Texas at Austin, December 2, 2009.
4. Shayak Banerjee, "Electrically-Driven Optical Proximity Correction and Applications," Electrical and Computer Engineering, The University of Texas at Austin, May 15, 2009.
3. Mark McDermott, "Cognitive Sensor Platform," Electrical and Computer Engineering, The University of Texas at Austin, May 1, 2009.
2. Sriram Sambamurthy, "Power Estimation of Microprocessors," Electrical and Computer Engineering, The University of Texas at Austin, December 1, 2008.
1. Pramod Chandraiah, "Source Re-Coder for SoC Specification Development," Electrical Engineering and Computer Science, University of California, Irvine, September 6, 2005.

M.S. Thesis Committee Member

10. Sreenivaas Muthyala Sudhakar, "Improving Encoding Efficiency in Test Compression using Sequential Linear Decompressors with Retained Free Variables," Electrical and Computer Engineering, The University of Texas at Austin, May 2013.
9. Donald E. Owen Jr., "The Feasibility of Memory Encryption and Authentication," Electrical and Computer Engineering, The University of Texas at Austin, April 2013.
8. Gaurav Nolkha, "Scaling and Improving Mapping of Module Level Vectors to Software Based Self Tests," Electrical and Computer Engineering, The University of Texas at Austin, May 2009.
7. Eric James Johnson, "Efficient Debugging and Tracing of System Level Designs," Electrical and Computer Engineering, University of California, Irvine, March 2006.
6. Alexander Gluhak, "Development of a Graphical User Interface for a System-On-Chip Design Environment" (in German), Electrical Engineering and Information Technology, University of Applied Sciences, Offenburg, Germany, April 2002.
5. David Berner, "Development of a Visual Refinement and Exploration Tool for SpecC," Electrical Engineering and Information Technology, University of Applied Sciences, Offenburg, Germany, March 2001.
4. Martin von Weymarn, "Development of a Specification Model of the EFR Vocoder," Institute of Computer and Communication Network Engineering, Technical University of Braunschweig, Germany, July 2001.

M.S. Report Committee Member

3. Matthew C. Slowik, "A Flexible Display System for Embedded Applications," Master of Science in Engineering, The University of Texas at Austin, April 2013.
2. Hans L. Yaeger, "Microprocessor Power Management and a Stand-alone Benchmarking Application for Android Based Platforms," Master of Science in Engineering, The University of Texas at Austin, December 2011.
1. Thomas G. Madaelil, "Clock Gating for Floating Point Units," Master of Science in Engineering, The University of Texas at Austin, December 2009.

Senior Design Projects Mentored

2. Kevin Johns, Andy Kaplan, Martin Lin, Ali Mohandesi, and Justin Prukop, "Digital Post-It Note," Electrical and Computer Engineering, The University of Texas at Austin, August 2012-May 2013.
1. Victor Azurin, Robert Graham, Maykel Hanna, Mina Hanna, and Shantu Jain, "MRI Simulation," Electrical and Computer Engineering, The University of Texas at Austin, August 2011-May 2012.

March 27, 2012

On March 26, I reviewed with Andreas about visiting his class and the general processing of the annual teaching review.

From 2-3:30 March 27, I sat in on his EE319K class in CPE2.206. Before class he engaged in friendly and informal discussions with students in the first two rows. This classroom has a central screen-projector and a tiny blackboard (no whiteboard).

He started with announcements. His voice is strong and articulate. He gave a vision of future labs

He posted the results of an exam from last week, and explained the rationale and grading policies. This was very difficult because the class average was low. He overviewed how the students should have approached the exam. In particular, he how to design software (correctness of the software, execution speed, space it requires.)

He talked about making a plan (flowcharts). Defined complexity as the number of steps. He showed the number of steps to find primes as (n-1)n/2. Algorithm development, implementation, and testing.

Comment: as you stand and talk (plan, algorithm, implementation, testing) from slides... students could not take notes. Repeat student's questions. Excess word "right"

He discussed recursion, using Codepad on the screen, and also used the black board. This was effective... even when he made programming mistakes. He discussed both the natural and efficient solutions of factorial and Fibonacci.

He discussed printing decimal numbers; he showed many versions; hard coded, iterative, and recursion. He as very effective using codepad to show software development. He made nice reference to earlier discussion of algorithms.

Reviewed I/O synchronization from a previous lecture. He had an effective analogy with communicating with a "hardware student", describing blind, polling and interrupts. He gave a nice introduction to interrupts. He had a good comparison of timer wait (polling) and periodic timer interrupts.

The students were very engaged, with lots of questions.

Jon Valvano

To: Ahmed Tewfik, Chairman, ECE
From: Yale Patt
Subject: Peer Evaluation of Andreas Gerstlauer's teaching.
Date: March 28, 2013

I attended Professor Andreas Gerstlauer's class in EE 319K on March 26 for the purpose of evaluating his teaching, as part of our Peer Teaching Evaluaton program. I met with Andreas before the class to review the process with him. I also met with him afterward to provide feedback on what I observed and answer his questions.

The class essentially had three parts to it: review hints for an upcoming midterm exam, insights into a lab experiment that the students were doing concurrently, and the lecture on new material. This could have resulted in a very dijointed presentation, but it did not. Professor Gerstlauer has a very comfortable classroom manner that allowed him to move easily from topic to topic without giving the feeling of disjointedness.

The lecture material treated three topics: Merge sort, Digital to Analog Converters and the notion of Sound. I will comment on each.

Merge sort. Professor Gerstlauer used the merge sort to shed insights into recursion and divide and conquer algorithms. He used the whiteboard to show an overview of merge sort, combined with a laptop computer for generating the actual merge sort code. I was frankly impressed with how skillfully he moved from one medium to the other, continually keeping his eye on the class so as to never lose contact with them.

Two things I was disappointed in this presentation: (1) he did not use the opportunity to mention the potential for parallelism which is inherent in merge sort and (2) he did not actually run the program he typed. We discussed both in my meeting with him afterward. In the case of parallelism, he was concerned that if he did mention it, he would be introducing too many concepts at the same time, and parallelism was not central to the points he was trying to get across in that lecture. In the case of running the code he typed, he was conscious of the amount of class time he had available. Both explanations are reasonable.

Digital Analog Conversion (DAC). Professor Gerstlauer started with the fundamentals, in this case the voltage divider. He showed how to get a voltage between 0 volts and a maximum voltage (in his case, 3.2 volts) with the voltage divider. Two things I liked about this part of his lecture: (1) He emphasized fundamentals (e.g., Ohm's Law, and Kirchoff's Current Law). (2) He started small, illustrating the priniple, and then built larger structures. He designed a 2-bit DAC and then moved on to a 4-bit DAC. Both techniques I felt contributed to the students understanding the material. He emphasized important points and repeated them. Again, I thought his combined use of .ppt and whiteboard was excellent. For example, on his .ppt slide he had bullets (e.g., linearity, monotonic). He went to the white board to illustrate what each bullet meant. Also, he showed on the white board what it means to be non-monotonic, and non-linear. I think this is very important to the explanation of a new concept: telling the student not only what it is, but also what it is not.

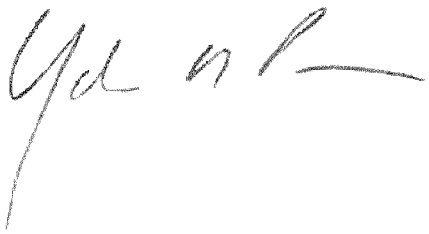
The last step in his treatment of DAC was the use of its output. Here, the essential issue is the loading due to the next stage which uses the DAC output as its input. Here he pointed out why the voltage divider did not give quite the voltage he earlier computed. I would have preferred him to mention infinite impedance when he first derived the voltage divider equations, with a comment that in reality the impedance is not infinite as they will see later in the lecture when he discusses using the output of the DAC. However, this criticism is a very minor point, and in fact, not all teachers believe the use of forward pointers is a good idea. We discussed this in our meeting after his lecture.

He concluded his treatment of DAC with an invitation to the students to build a 16-bit DAC if they wished, with a smile and the words: "Be my guest!" I thought this simple statement was indicative of the comfortable rapport he had with the class.

Sound: The final topic he taught in lecture was the notion of sound. Professor Gerstlauer related this well to the human ear: amplitude, pitch, and duration (tempo). He discussed the waveforms produced by different musical instruments, and the notion of a chord. In short, he built up music from the starting point of a single sine wave, adding complexity as he felt necessary.

The only negative comment I saw in the lecture was that not everyone was engaged. Some students spent the entire lecture surfing the web on their laptops. We discussed this in our meeting after the lecture. He is bothered by this but does not what to do about it. Actually, we all suffer from this problem to some extent, that if students are surfing the web, they are not paying attention to what is going on in class, and if they are not paying attention, they can not learn. The excuse for allowing students to have their laptops open is their claim they use the laptop to take notes. Since I did not see anyone using the laptop to take notes, one suggestion is he simply insist that all laptops be turned off at the start of class. As I said, this problem is not unique to Professor Gerstlauer.

Bottom line: I thought Professor Gerstlauer did an excellent job in the lecture I observed. He clearly wanted his students to learn. He had a comfortable manner, kept most of the students engaged, moved effortlessly between laptop, .ppt, and whiteboard, gave clear explanations, and developed his treatment in straightforward fashion, starting with simple structures and systematically building more and more complicated ones. It was a pleasure for me to observe this class.



Summary of Recent (All Years In Rank) UT Austin Course-Instructor Survey Resul
Overall Course/Instructor Items

Semester	Course Number	Course Title	Enrollment		Instructor Averages*		College/School Averages**		
			No. of Students Enrolled on 12th Class Day	No. of Surveys Returned at End of Semester	Overall Instructor Rating Avg.	Overall Course Rating Avg.	Overall Instructor Rating Avg.	Overall Course Rating Avg.	No. Classes Surveyed
Fall 08	E E 382V	EMBEDDED SYS DSGN AND MODELING	19	16	4.4	3.8	N/A ***	N/A ***	N/A
Spring 09	E E 319K	INTRO TO MICROCONTROLLERS	16	21	4.1	4.2	N/A ***	N/A ***	N/A
Fall 09	E E 382V	EMBEDDED SYS DSGN AND MODELING	26	24	3.8	3.5	N/A ***	N/A ***	N/A
Spring 10	E E 382V	SYSTEM-ON-A-CHIP DESIGN	18	15	4.6	4.3	N/A ***	N/A ***	N/A
Fall 10	E E 382V	EMBEDDED SYS DSGN AND MODELING	15	14	4.1	3.9	N/A ***	N/A ***	N/A
Spring 11	E E 319K	INTRO TO EMBEDDED SYSTEMS	84	26	3.7	3.3	N/A ***	N/A ***	N/A
Spring 11	E E 382V	SYSTEM-ON-A-CHIP DESIGN	10	10	4.2	3.6	N/A ***	N/A ***	N/A
Fall 11	E E 999W	DISSERTATION	1	1	5.0	5.0	N/A ***	N/A ***	N/A
Fall 11	E E 382V	EMBEDDED SYS DSGN AND MODELING	14	13	4.5	3.9	N/A ***	N/A ***	N/A
Spring 12	E E 319K	INTRO TO EMBEDDED SYSTEMS	73	59	4.3	3.7	N/A ***	N/A ***	N/A
Fall 12	E E 382V	SYSTEM-ON-A-CHIP DESIGN	41	31	4.2	3.7	N/A ***	N/A ***	N/A
Spring 13	E E 319K	INTRO TO EMBEDDED SYSTEMS	71	35	4.1	3.9	N/A ***	N/A ***	N/A

*For the computation of the averages, points were assigned to student responses as follows:
Excellent = 5, Very Good = 4, Satisfactory = 3, Unsatisfactory = 2, Very Unsatisfactory = 1

**College/school averages are the average of class averages, based on all courses surveyed in the instructor's college or school during the academic year in which the course was taught.

***New CIS forms were implemented in the fall 2000 semester. The average rating on the overall course and instructor questions on the new Basic and Expanded forms have been found to be approximately 0.1 to 0.2 points lower than those ratings on the old Common form.

Prepared by the Measurement and Evaluation Center

*** PROVISIONAL REPORT ***

UNIVERSITY OF TEXAS AT AUSTIN
Gerstlauer, Andreas M E E319K 16165
B000 Basic
SURVEYED WITH: 16170 16175 16180

COURSE-INSTRUCTOR SURVEY
INTRO TO EMBEDDED SYSTEMS

Spring 2013 DEPARTMENT COPY
Enrollment = 68
Surveys Returned = 35

	NUMBER CHOOSING EACH RESPONSE					NO. REPLIES THIS ITEM	AVG.
	Str Disag	Disagree	Neutral	Agree	Str Agree		
1 COURSE WELL-ORGANIZED	0	2	4	16	13	35	4.1
2 COMMUNICATED INFORMATION EFFECTIVELY	0	2	5	15	13	35	4.1
3 SHOWED INTEREST IN STUDENT PROGRESS	0	0	4	18	13	35	4.3
4 ASSIGNMENTS AND TESTS RETURNED PROMPTLY	0	0	1	15	19	35	4.5
5 STUDENT FREEDOM OF EXPRESSION	0	0	2	16	17	35	4.4
6 COURSE OF VALUE TO DATE	1	0	3	13	18	35	4.3
	Vry Unsat	Unsat	Satisfact	Very Good	Excellent		
7 OVERALL INSTRUCTOR RATING	0	1	7	15	12	35	4.1
8 OVERALL COURSE RATING	1	1	7	19	7	35	3.9
	Excessive	High	Average	Light	Insuffic		
9 STUDENT RATING OF COURSE WORKLOAD	9	22	2	0	1	34	
	Less 2.00	2.00-2.49	2.50-2.99	3.00-3.49	3.50-4.00		
10 OVERALL UT GRADE POINT AVERAGE	1	0	12	10	11	34	
	A	B	C	D	F		
11 PROBABLE COURSE GRADE	13	17	3	0	0	33	

For the computation of averages, values were assigned on a 5-point scale so that the most favorable response was assigned a value of 5 and the least favorable response was assigned a value of 1.

Scanned: 06/06/2013 Printed: 06/26/2013

UNIVERSITY OF TEXAS AT AUSTIN
Gerstlauer, Andreas M E E382V 17070
8000 Basic

COURSE-INSTRUCTOR SURVEY
SYSTEM-ON-A-CHIP DESIGN

Fall 2012 DEPARTMENT COPY
Enrollment = 41
Surveys Returned = 31

	NUMBER CHOOSING EACH RESPONSE					NO. REPLIES THIS ITEM	AVG.
	Str Disag	Disagree	Neutral	Agree	Str Agree		
1 COURSE WELL-ORGANIZED	0	2	4	13	11	30	4.1
2 COMMUNICATED INFORMATION EFFECTIVELY	0	0	2	14	15	31	4.4
3 SHOWED INTEREST IN STUDENT PROGRESS	0	0	1	12	18	31	4.5
4 ASSIGNMENTS AND TESTS RETURNED PROMPTLY	0	0	4	11	15	30	4.4
5 STUDENT FREEDOM OF EXPRESSION	0	0	1	14	15	30	4.5
6 COURSE OF VALUE TO DATE	0	3	4	18	6	31	3.9
	Vry Unsat	Unsat	Satisfact	Very Good	Excellent		
7 OVERALL INSTRUCTOR RATING	0	0	6	14	11	31	4.2
8 OVERALL COURSE RATING	0	3	9	13	6	31	3.7
	Excessive	High	Average	Light	Insuffic		
9 STUDENT RATING OF COURSE WORKLOAD	4	17	9	0	0	30	
	Less 2.00	2.00-2.49	2.50-2.99	3.00-3.49	3.50-4.00		
10 OVERALL UT GRADE POINT AVERAGE	0	0	0	5	16	21	
	A	B	C	D	F		
11 PROBABLE COURSE GRADE	15	14	0	0	0	29	

For the computation of averages, values were assigned on a 5-point scale so that the most favorable response was assigned a value of 5 and the least favorable response was assigned a value of 1.

Scanned: 01/28/2013

Printed: 02/19/2013

Student comments (if available):

UNIVERSITY OF TEXAS AT AUSTIN
Gerstlauer, Andreas M E E319K 16275
BGOO Basic
SURVEYED WITH: 16280 16285 16290

COURSE-INSTRUCTOR SURVEY
INTRO TO EMBEDDED SYSTEMS

Spring 2012 DEPARTMENT COPY
Enrollment = 70
Surveys Returned = 59

	NUMBER CHOOSING EACH RESPONSE					NO. REPLIES THIS ITEM	AVG.
	Str Disag	Disagree	Neutral	Agree	Str Agree		
1 COURSE WELL-ORGANIZED	1	1	6	33	18	59	4.1
2 COMMUNICATED INFORMATION EFFECTIVELY	0	0	5	33	21	59	4.3
3 SHOWED INTEREST IN STUDENT PROGRESS	0	0	1	21	37	59	4.6
4 ASSIGNMENTS AND TESTS RETURNED PROMPTLY	0	0	3	27	29	59	4.4
5 STUDENT FREEDOM OF EXPRESSION	0	0	2	19	38	59	4.6
6 COURSE OF VALUE TO DATE	0	2	1	21	34	58	4.5
	Vry Unsat	Unsat	Satisfact	Very Good	Excellent		
7 OVERALL INSTRUCTOR RATING	0	0	7	28	24	59	4.3
8 OVERALL COURSE RATING	0	1	27	18	13	59	3.7
	Excessive	High	Average	Light	Insuffic		
9 STUDENT RATING OF COURSE WORKLOAD	22	29	6	1	1	59	
	Less 2.00	2.00-2.49	2.50-2.99	3.00-3.49	3.50-4.00		
10 OVERALL UT GRADE POINT AVERAGE	1	1	14	22	21	59	
	A	B	C	D	F		
11 PROBABLE COURSE GRADE	16	33	9	1	0	59	

For the computation of averages, values were assigned on a 5-point scale so that the most favorable response was assigned a value of 5 and the least favorable response was assigned a value of 1.

Scanned: 05/24/2012

Printed: 07/17/2012

Student comments (if available):

UNIVERSITY OF TEXAS AT AUSTIN — COURSE-INSTRUCTOR SURVEY — Fall 2011 DEPARTMENT COPY
Gerstlauer, Andreas M E E382V 17190 — EMBEDDED SYS DSGN AND MODELING — Enrollment = 14
B000 Basic — Surveys Returned = 13

	NUMBER CHOOSING EACH RESPONSE					NO. REPLIES THIS ITEM	AVG.
	Str Disag	Disagree	Neutral	Agree	Str Agree		
1 COURSE WELL-ORGANIZED	0	0	2	7	4	13	4.2
2 COMMUNICATED INFORMATION EFFECTIVELY	0	0	1	4	8	13	4.5
3 SHOWED INTEREST IN STUDENT PROGRESS	0	0	0	4	9	13	4.7
4 ASSIGNMENTS AND TESTS RETURNED PROMPTLY	0	0	0	7	6	13	4.5
5 STUDENT FREEDOM OF EXPRESSION	0	0	0	4	9	13	4.7
6 COURSE OF VALUE TO DATE	0	0	1	6	6	13	4.4
	Vry Unsat	Unsat	Satisfact	Very Good	Excellent		
7 OVERALL INSTRUCTOR RATING	0	0	1	4	8	13	4.5
8 OVERALL COURSE RATING	0	1	1	9	2	13	3.9
	Excessive	High	Average	Light	Insuffic		
9 STUDENT RATING OF COURSE WORKLOAD	0	3	9	1	0	13	
	Less 2.00	2.00-2.49	2.50-2.99	3.00-3.49	3.50-4.00		
10 OVERALL UT GRADE POINT AVERAGE	0	0	0	3	7	10	
	A	B	C	D	F		
11 PROBABLE COURSE GRADE	10	2	0	0	0	12	

For the computation of averages, values were assigned on a 5-point scale so that the most favorable response was assigned a value of 5 and the least favorable response was assigned a value of 1.

Scanned: 12/20/2011 Printed: 07/16/2012

Student comments (if available):

UNIVERSITY OF TEXAS AT AUSTIN
Gerstlauer, Andreas M E E382V 17075
8000 Basic

COURSE-INSTRUCTOR SURVEY
SYSTEM-ON-A-CHIP DESIGN

Spring 2011 DEPARTMENT COPY
Enrollment = 10
Surveys Returned = 10

	NUMBER CHOOSING EACH RESPONSE					NO. REPLIES THIS ITEM	AVG.
	Str Disag	Disagree	Neutral	Agree	Str Agree		
1 COURSE WELL-ORGANIZED	0	0	0	8	2	10	4.2
2 COMMUNICATED INFORMATION EFFECTIVELY	0	0	0	7	3	10	4.3
3 SHOWED INTEREST IN STUDENT PROGRESS	0	0	0	5	5	10	4.5
4 ASSIGNMENTS AND TESTS RETURNED PROMPTLY	0	0	0	3	7	10	4.7
5 STUDENT FREEDOM OF EXPRESSION	0	0	0	2	8	10	4.8
6 COURSE OF VALUE TO DATE	0	0	0	5	5	10	4.5
	Vry Unsat	Unsat	Satisfact	Very Good	Excellent		
7 OVERALL INSTRUCTOR RATING	0	0	1	6	3	10	4.2
8 OVERALL COURSE RATING	0	0	4	6	0	10	3.6
	Excessive	High	Average	Light	Insuffic		
9 STUDENT RATING OF COURSE WORKLOAD	1	7	2	0	0	10	
	Less 2.00	2.00-2.49	2.50-2.99	3.00-3.49	3.50-4.00		
10 OVERALL UT GRADE POINT AVERAGE	0	0	0	1	9	10	
	A	B	C	D	F		
11 PROBABLE COURSE GRADE	7	1	0	0	0	8	

For the computation of averages, values were assigned on a 5-point scale so that the most favorable response was assigned a value of 5 and the least favorable response was assigned a value of 1.

Scanned: 05/19/2011

Printed: 09/11/2012

Student comments (if available):

UNIVERSITY OF TEXAS AT AUSTIN
Gerstlauer, Andreas M E E319K 16305
8000 Basic
SURVEYED WITH: 16310 16315 16353

COURSE-INSTRUCTOR SURVEY
INTRO TO EMBEDDED SYSTEMS

Spring 2011 DEPARTMENT COPY
Enrollment = 78
Surveys Returned = 26

	NUMBER CHOOSING EACH RESPONSE					NO. REPLIES THIS ITEM	AVG.
	Str Disag	Disagree	Neutral	Agree	Str Agree		
1 COURSE WELL-ORGANIZED	1	1	3	16	5	26	3.9
2 COMMUNICATED INFORMATION EFFECTIVELY	0	2	9	9	6	26	3.7
3 SHOWED INTEREST IN STUDENT PROGRESS	0	0	4	15	7	26	4.1
4 ASSIGNMENTS AND TESTS RETURNED PROMPTLY	0	0	0	18	8	26	4.3
5 STUDENT FREEDOM OF EXPRESSION	0	2	2	14	8	26	4.1
6 COURSE OF VALUE TO DATE	0	0	3	13	10	26	4.3
	Vry Unsat	Unsat	Satisfact	Very Good	Excellent		
7 OVERALL INSTRUCTOR RATING	0	3	9	7	7	26	3.7
8 OVERALL COURSE RATING	2	3	10	8	3	26	3.3
	Excessive	High	Average	Light	Insuffic		
9 STUDENT RATING OF COURSE WORKLOAD	12	10	3	1	0	26	
	Less 2.00	2.00-2.49	2.50-2.99	3.00-3.49	3.50-4.00		
10 OVERALL UT GRADE POINT AVERAGE	0	2	4	5	15	26	
	A	B	C	D	F		
11 PROBABLE COURSE GRADE	6	15	5	0	0	26	

For the computation of averages, values were assigned on a 5-point scale so that the most favorable response was assigned a value of 5 and the least favorable response was assigned a value of 1.

Student comments (if available):

UNIVERSITY OF TEXAS AT AUSTIN
Gerstlauer, Andreas M E E382V 16985
B000 Basic

COURSE-INSTRUCTOR SURVEY
EMBEDDED SYS DSGN AND MODELING

Fall 2010 DEPARTMENT COPY
Enrollment = 15
Surveys Returned = 14

	NUMBER CHOOSING EACH RESPONSE					NO. REPLIES THIS ITEM	AVG.
	Str Disag	Disagree	Neutral	Agree	Str Agree		
1 COURSE WELL-ORGANIZED	0	0	0	7	7	14	4.5
2 COMMUNICATED INFORMATION EFFECTIVELY	0	0	0	7	7	14	4.5
3 SHOWED INTEREST IN STUDENT PROGRESS	0	0	0	10	4	14	4.3
4 ASSIGNMENTS AND TESTS RETURNED PROMPTLY	0	0	0	8	6	14	4.4
5 STUDENT FREEDOM OF EXPRESSION	0	0	0	4	10	14	4.7
6 COURSE OF VALUE TO DATE	0	0	5	5	4	14	3.9
	Vry Unsat	Unsat	Satisfact	Very Good	Excellent		
7 OVERALL INSTRUCTOR RATING	0	0	2	8	4	14	4.1
8 OVERALL COURSE RATING	0	0	5	6	3	14	3.9
	Excessive	High	Average	Light	Insuffic		
9 STUDENT RATING OF COURSE WORKLOAD	0	8	6	0	0	14	
	Less 2.00	2.00-2.49	2.50-2.99	3.00-3.49	3.50-4.00		
10 OVERALL UT GRADE POINT AVERAGE	0	0	0	2	8	10	
	A	B	C	D	F		
11 PROBABLE COURSE GRADE	9	4	0	0	0	13	

For the computation of averages, values were assigned on a 5-point scale so that the most favorable response was assigned a value of 5 and the least favorable response was assigned a value of 1.

Scanned: 12/10/2010

Printed: 06/24/2013

Student comments (if available):

*** PROVISIONAL REPORT ***

UNIVERSITY OF TEXAS AT AUSTIN — COURSE-INSTRUCTOR SURVEY — Spring 2010 DEPARTMENT COPY
Garstlauer, Andreas M E E382V 16835 — SYSTEM-ON-A-CHIP DESIGN — Enrollment = 18
B000 Basic — Surveys Returned = 15

	NUMBER CHOOSING EACH RESPONSE					NO. REPLIES THIS ITEM	AVG.
	Str Disag	Disagree	Neutral	Agree	Str Agree		
1 COURSE WELL-ORGANIZED	0	0	0	8	7	15	4.5
2 COMMUNICATED INFORMATION EFFECTIVELY	0	0	0	4	11	15	4.7
3 SHOWED INTEREST IN STUDENT PROGRESS	0	0	0	3	12	15	4.8
4 ASSIGNMENTS AND TESTS RETURNED PROMPTLY	0	0	0	4	11	15	4.7
5 STUDENT FREEDOM OF EXPRESSION	0	0	0	3	12	15	4.8
6 COURSE OF VALUE TO DATE	0	0	0	7	8	15	4.5
	Vry Unsat	Unsat	Satisfact	Very Good	Excellent		
7 OVERALL INSTRUCTOR RATING	0	0	0	6	9	15	4.6
8 OVERALL COURSE RATING	0	0	2	7	6	15	4.3
	Excessive	High	Average	Light	Insuffic		
9 STUDENT RATING OF COURSE WORKLOAD	0	9	5	1	0	15	
	Less 2.00	2.00-2.49	2.50-2.99	3.00-3.49	3.50-4.00		
10 OVERALL UT GRADE POINT AVERAGE	0	0	0	2	12	14	
	A	B	C	D	F		
11 PROBABLE COURSE GRADE	10	4	0	0	0	14	

For the computation of averages, values were assigned on a 5-point scale so that the most favorable response was assigned a value of 5 and the least favorable response was assigned a value of 1.

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*** PROVISIONAL REPORT ***

UNIVERSITY OF TEXAS AT AUSTIN — COURSE-INSTRUCTOR SURVEY — Fall 2009 DEPARTMENT COPY
Gerstlauer, Andreas M E E382V 17220 — EMBEDDED SYS DSGN AND MODELING — Enrollment = 28
8000 Basic — Surveys Returned = 24

	NUMBER CHOOSING EACH RESPONSE					NO. REPLIES THIS ITEM	AVG.
	Str Disag	Disagree	Neutral	Agree	Str Agree		
1 COURSE WELL-ORGANIZED	0	2	2	14	6	24	4.0
2 COMMUNICATED INFORMATION EFFECTIVELY	0	1	2	13	8	24	4.2
3 SHOWED INTEREST IN STUDENT PROGRESS	0	1	2	13	8	24	4.2
4 ASSIGNMENTS AND TESTS RETURNED PROMPTLY	0	1	2	13	8	24	4.2
5 STUDENT FREEDOM OF EXPRESSION	0	1	0	13	10	24	4.3
6 COURSE OF VALUE TO DATE	0	2	4	14	4	24	3.8
	Vry Unsat	Unsat	Satisfact	Very Good	Excellent		
7 OVERALL INSTRUCTOR RATING	0	0	9	11	4	24	3.8
8 OVERALL COURSE RATING	0	2	11	8	3	24	3.5
	Excessive	High	Average	Light	Insuffic		
9 STUDENT RATING OF COURSE WORKLOAD	1	11	10	1	0	23	
	Less 2.00	2.00-2.49	2.50-2.99	3.00-3.49	3.50-4.00		
10 OVERALL UT GRADE POINT AVERAGE	0	0	0	2	13	15	
	A	B	C	D	F		
11 PROBABLE COURSE GRADE	8	14	0	0	0	22	

For the computation of averages, values were assigned on a 5-point scale so that the most favorable response was assigned a value of 5 and the least favorable response was assigned a value of 1.

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*** PROVISIONAL REPORT ***

UNIVERSITY OF TEXAS AT AUSTIN
Gerstlauer, Andreas M E E319K 15965
B000 Basic

COURSE-INSTRUCTOR SURVEY
INTRO TO MICROCONTROLLERS

Spring 2009 DEPARTMENT COPY
Enrollment = 16
Surveys Returned = 21

	NUMBER CHOOSING EACH RESPONSE					NO. REPLIES THIS ITEM	AVG.
	Str Disag	Disagree	Neutral	Agree	Str Agree		
1 COURSE WELL-ORGANIZED	0	0	1	10	10	21	4.4
2 COMMUNICATED INFORMATION EFFECTIVELY	0	0	3	10	8	21	4.2
3 SHOWED INTEREST IN STUDENT PROGRESS	0	0	3	9	9	21	4.3
4 ASSIGNMENTS AND TESTS RETURNED PROMPTLY	0	0	0	11	10	21	4.5
5 STUDENT FREEDOM OF EXPRESSION	0	0	2	9	10	21	4.4
6 COURSE OF VALUE TO DATE	0	0	0	7	14	21	4.7
	Vry Unsat	Unsat	Satisfact	Very Good	Excellent		
7 OVERALL INSTRUCTOR RATING	0	0	4	11	6	21	4.1
8 OVERALL COURSE RATING	0	0	3	11	7	21	4.2
	Excessive	High	Average	Light	Insuffic		
9 STUDENT RATING OF COURSE WORKLOAD	2	12	7	0	0	21	
	Less 2.00	2.00-2.49	2.50-2.99	3.00-3.49	3.50-4.00		
10 OVERALL UT GRADE POINT AVERAGE	0	4	5	6	6	21	
	A	B	C	D	F		
11 PROBABLE COURSE GRADE	13	5	3	0	0	21	

For the computation of averages, values were assigned on a 5-point scale so that the most favorable response was assigned a value of 5 and the least favorable response was assigned a value of 1.

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*** PROVISIONAL REPORT ***

UNIVERSITY OF TEXAS AT AUSTIN — COURSE-INSTRUCTOR SURVEY — Fall 2008 DEPARTMENT COPY
Gerstlauer, Andreas M E E382V 17295 — EMBEDDED SYS DSGN AND MODELING — Enrollment = 19
8000 Basic — Surveys Returned = 16

	NUMBER CHOOSING EACH RESPONSE					NO. REPLIES THIS ITEM	AVG.
	Str Disag	Disagree	Neutral	Agree	Str Agree		
1 COURSE WELL-ORGANIZED	0	0	2	8	6	16	4.3
2 COMMUNICATED INFORMATION EFFECTIVELY	0	0	1	5	10	16	4.6
3 SHOWED INTEREST IN STUDENT PROGRESS	0	0	0	3	13	16	4.8
4 ASSIGNMENTS AND TESTS RETURNED PROMPTLY	0	0	1	7	8	16	4.4
5 STUDENT FREEDOM OF EXPRESSION	0	0	0	4	12	16	4.8
6 COURSE OF VALUE TO DATE	0	0	2	6	8	16	4.4
	Vry Unsat	Unsat	Satisfact	Very Good	Excellent		
7 OVERALL INSTRUCTOR RATING	0	0	1	7	8	16	4.4
8 OVERALL COURSE RATING	0	0	5	9	2	16	3.8
	Excessive	High	Average	Light	Insuffic		
9 STUDENT RATING OF COURSE WORKLOAD	1	8	7	0	0	16	
	Less 2.00	2.00-2.49	2.50-2.99	3.00-3.49	3.50-4.00		
10 OVERALL UT GRADE POINT AVERAGE	0	0	0	2	11	13	
	A	B	C	D	F		
11 PROBABLE COURSE GRADE	11	4	0	0	0	15	

For the computation of averages, values were assigned on a 5-point scale so that the most favorable response was assigned a value of 5 and the least favorable response was assigned a value of 1.

Scanned: 12/09/2008 Printed: 12/09/2008

THE UNIVERSITY OF TEXAS AT AUSTIN
OFFICE OF GRADUATE STUDIES
COMMITTEE REPORT, MASTERS AND DOCTORAL
FOR GERSTLAUER, ANDREAS M

NAME	EID	LAST SEM	COMM POSITION	MAST OR DOCT	DEGREE	FIELD	YYS	2ND DEGREE	FIELD	YYS
ABDEL HADI, AHMED MOHAMED	ama2875	119	CO-CHAIR	D	PH.D.	ELECTRICAL AN	20119			
ANGEPAT, HARI DAAS	hda73	132	MEMBER	D						
ARNDT, KARL ROBERT	kra469	109	MEMBER	M	M.S.E.	ELECTRICAL AN	20109			
BANERJEE, SHAYAK	sb4399	102	MEMBER	D	PH.D.	ELECTRICAL AN	20102			
BHARGAVA, VIDUR	vb723	139	MEMBER	D						
CHAUDHARI, AMEYA SUHAS	asc835	139	MEMBER	D						
DATTA, RUDRAJIT	rd8658	119	MEMBER	D	PH.D.	ELECTRICAL AN	20119			
GOSWAMI, ARINDAM	ag36423	116	CHAIR	M	M.S.E.	ELECTRICAL AN	20116			
HE, KU	kh22582	122	CO-CHAIR	D	PH.D.	ELECTRICAL AN	20122			
IQBAL, MUHAMMAD FAISAL	mi622	136	MEMBER	D	PH.D.	ELECTRICAL AN	20136			
JANG, WOO YOUNG	wyj59	112	MEMBER	D	PH.D.	ELECTRICAL AN	20112			
KATHURIA, MANAN	mk22928	122	CHAIR	M	M.S.E.	ELECTRICAL AN	20122			
KRIMER, EVGENI	ek4559	122	MEMBER	D	PH.D.	ELECTRICAL AN	20122			
MADAELIL, THOMAS G.	madaelil	099	MEMBER	M	M.S.E.	ELECTRICAL AN	20099			
MCDERMOTT, MARK WILLIAM	mcdermot	139	MEMBER	D						
MIAO, JIN	jm58482	139	CO-CHAIR	D						
MIAO, JIN	jm58482	139	CO-CHAIR	M	M.S.E.	ELECTRICAL AN	20129			
MUTHYALA SUDHAKAR, S.	sm45346	139	MEMBER	M	M.S.E.	ELECTRICAL AN	20132			
NOLKHA, GAURAV	gn2456	092	MEMBER	M	M.S.E.	ELECTRICAL AN	20092			
OVERHOLT, PETER JAMES	pjo268	096	CHAIR	M	M.S.E.	ELECTRICAL AN	20096			
OWEN, DONALD EDWARD JR	deo248	132	MEMBER	M	M.S.E.	ELECTRICAL AN	20132			
PAINE, NICHOLAS ARDEN	nap244	136	MEMBER	D						
PATIL, NIKHIL AJAY	nap343	139	MEMBER	D						
PEDRAM, ARDAVAN	ap7437	136	CHAIR	D	PH.D.	ELECTRICAL AN	20136			

NAME	EID	LAST SEM	COMM POSITION	MAST OR DOCT	DEGREE	FIELD	YYS	2ND DEGREE	FIELD	YYS
PFEIFER, DYLAN CONRAD	dcp73	136	CO-CHAIR	D						
PRABHU, MAHESH	mp24482	139	MEMBER	D						
RAB, MUHAMMAD TAUSEEF	rabmt	132	MEMBER	D	PH.D.	ELECTRICAL AN	20132			
RAZAGHI, PARISA	pr6689	139	CHAIR	D						
RHU, MINSOO	mr35987	139	MEMBER	D						
SALINAS BOMFIM, PABLO E.	pes478	102	CHAIR	M	M.S.E.	ELECTRICAL AN	20102			
SAMBAMURTHY, SRIRAM	s2481986	106	MEMBER	D	PH.D.	ELECTRICAL AN	20106			
SINHA, ASHMITA	as49366	126	CHAIR	M	M.S.E.	ELECTRICAL AN	20126			
SLOWIK, MATTHEW CALDWELL	mcs2955	132	MEMBER	M	M.S.E.	ELECTRICAL AN	20132			
SOHN, JONGWOOK	js54957	132	MEMBER	D	PH.D.	ELECTRICAL AN	20132			
TOURISH, JOHN PATRICK	jpt642	112	CHAIR	M	M.S.E.	ELECTRICAL AN	20112			
WILLIAMS, JOEL THOMAS	jtw838	102	CHAIR	M	M.S.E.	ELECTRICAL AN	20102			
WU, GENE YING	wugy	139	MEMBER	D						
YEAGER, HANS L.	hly88	119	MEMBER	M	M.S.E.	ELECTRICAL AN	20119			

Postdoctoral fellows supervised: None

Budget Council Assessment on Research, Publications, and Other Evidence of Scholarship/Creativity for Andreas Gerstlauer

Introduction

This statement on Research, Publications, and Other Evidence of Scholarship/Creativity was prepared by Budget Council Members Jacob Abraham, Brian L. Evans and Yale N. Patt. It is based on a thorough evaluation of Dr. Gerstlauer's research, publications, grants, and international reputation, as well as our own knowledge of his activities and research area.

Research Area and Contributions

Dr. Gerstlauer conducts research in design methods and tools for improving computing systems that are embedded in a variety of products, from consumer electronics to civilian spacecraft and military systems. His methods and tools provide assistance for teams of designers in making key decisions and automating the design of the entire computing system based on the design decisions, which is known as Electronic System-Level Design Automation. Using his methods and tools, designers can explore many alternate choices at different stages in the design process and quantify the impact of the decision on the entire computing system. This is in contrast to many previous research efforts that have optimized a subsystem only to find out later that the overall performance of the full system has degraded.

Dr. Gerstlauer's research in embedded systems and electronic system-level design automation can be divided into the following categories: host-compiled modeling and simulation, system compilation and synthesis, co-design of domain-specific cores and approximate computing. His work has been published in the top venues in the field, and has captured the attention of researchers in academia and in industry. The software that he and his students have written has been used by other research groups around the world and has stimulated much research. Each category is evaluated in more detail below.

Contribution #1: Host-Compiled Modeling and Simulation (key papers [C38] and [J6])

Dr. Gerstlauer's simulation work addresses the two critical measures that are always at odds: computing performance and energy consumption. It used to be that reducing energy consumption did not matter; it was all about maximizing computing performance. That is no longer the case. Energy constraints in modern and future systems make energy a first-class citizen. That does not mean performance is no longer an issue. Everyone wants higher performance, but only within the allowed energy budget.

Dr. Gerstlauer proposed models for the increasingly complex computing systems. Each processing chip contains multiple processing engines (cores), and each core competes for on-chip resources (e.g., bandwidth and energy). And, processors are realizing increasingly complicated applications.

His simulation work balances very nicely the two major competitive forces to modeling, simulation time and accuracy. The heart of the problem is the granularity of the modeling. There are many examples in the literature of fine grain modeling where accurate modeling is demonstrated, but the execution time for that simulation makes the modeling impractical. Conversely, there are many examples of large grain modeling where the simulation is fast, but the accuracy is not good enough to be meaningful. Dr. Gerstlauer has been able to achieve near real-time simulation speeds with greater than 95% accuracy.

In his work, a key component is a back annotation technique that annotates source code intended for execution in a target system with timing and power metrics. As simulation proceeds, annotations provide measures of system execution to the simulation kernel, which dynamically adjusts modeling granularity. One gets accuracy when needed and simulation speed when accuracy can safely not be compromised.

Contribution #2: System Compilation and Synthesis (key papers [J5] and [J7])

Before automatically generating the appropriate structures on the integrated circuit, current electronic design automation tools require the design to be specified in low-level detail using a hardware description language. Advances in integrated circuit technology now enable entire Systems-on-Chips (SoCs), and existing electronic design automation tools are unable to deal with the problem.

Dr. Gerstlauer has been a pioneer in developing high-level languages for SoCs, in developing high-level models to describe heterogeneous systems, and in formulating synthesis algorithms for: mapping high-level designs to integrated circuits. In particular, he has developed the algorithms for exploring the design space, and partitioning the design and mapping application steps to computation units in the SoC. He also developed techniques for generating the software necessary for operation of the SoC: the embedded operating system, the device drivers, inter-processor communication and application code.

Dr. Gerstlauer formulated a system-level synthesis methodology and a taxonomy for classification of system-level synthesis approaches. His October 2009 paper [J5] laid the groundwork for further research in this area, and has had more than 60 citations. He developed the System-on-Chip Environment (SCE) for the design of SoCs. This approach is being used by companies, including NEC and Toshiba, and a derivative of the tool is being sold and supported by a commercial entity.

He developed a complete solution to the problem of synthesizing application models to hardware and software for generic multiprocessor SoC architectures. This involves exploration of the design space and decision making for both computation and communication. He has demonstrated viability of his system on industry examples and published the results in several key conferences and in a recent archival paper [J7]. Dr. Gerstlauer's contributions to this important but difficult problem have given him international recognition, and he is well on his way to becoming one of the world leaders in system-level synthesis.

Contribution #3: Co-Design of Domain-Specific Cores (key papers [J9] and [C50])

As mentioned above, reducing energy consumption has replaced maximizing computing performance as the major problem to be addressed in designing computing systems today. A very powerful approach to reducing energy required for computations replaces general-purpose processors with special-purpose and custom processors. Dr. Gerstlauer has made significant contributions in this direction.

He developed simple customizations for matrix multiplication algorithms that are at the core of many scientific and other high-performance computing applications. He designed a dedicated "Linear Algebra Processor" that could be used to achieve high energy efficiency in high-performance and embedded computing. He showed that this processor could also be applied to other computations, including matrix factorization and fast Fourier transforms. His techniques, along with fine tuning of memory, resulted in orders of magnitude improvement in energy efficiency compared with computation on leading multicore CPUs. His results were presented in leading conferences in his area and in an archival version [J9]. The significance of this work is highlighted by the fact that, in less than 9 months after publication, the archival paper has already been cited 13 times. His work in this area should lead to improved algorithms and architectures that significantly reduce the energy requirements for a variety of applications.

Dr. Gerstlauer has recently applied his ideas to the field of computational biology, specifically the problem of stochastic simulation of biochemical reactions. His special-purpose processor exploits fine and coarse grain parallelism, and is able to support networks of more than a million species and reactions [C50]. Broadening his research to deal with difficult computational problems in other disciplines demonstrates his creativity, and this will further enhance his reputation and international recognition.

Contribution #4: Approximate Computing (key papers [J11] and [C44])

Reducing power consumption is critical for battery-powered products (e.g., smart phones), large-scale systems (e.g., server farms) and points between. Power is the square of voltage, divided by resistance. Reducing voltage levels reduces power consumption but also generates more errors in results. With faculty colleague Dr. Orshansky, Dr. Gerstlauer took a different approach. In some applications, answers degrade gradually as errors increase; hence, one can tradeoff accuracy for power. By accepting a very small amount of error [J11], Dr. Gerstlauer reduced power consumption for video compression by 70%. This research integrates circuit-level and algorithm-level approaches to enable approximate computing.

Using a more systematic approach, Dr. Gerstlauer redesigned circuits to produce approximate output at reduced complexity and hence, energy. Adders and multipliers have stages of circuits implementing digital logic operations of NAND and NOR. With Dr. Orshansky, Dr. Gerstlauer has redesigned adders and multipliers to provide optimal quality-energy tradeoffs [C44]. At each point in the tradeoff curve, no other solution has higher quality for the same energy or lower energy for the same quality. Such a curve is known as Pareto optimal. This approach could be integrated into electronic design automation tools.

Publications

Dr. Gerstlauer has a very strong publication track record. As an Assistant Professor, he has published 9 journal papers, 32 peer-reviewed conference papers, and 1 book. (In his career, he has published 12 journal papers, 54 peer-reviewed conference papers, and 4 books.) In the research fields of embedded systems and electronic system-level design automation, both journals and top-tier conferences serve as the appropriate terminal peer-reviewed publication venues for major research contributions. Publishing in these top-tier conferences, which are well attended by academia and industry, attracts a lot of visibility and is extremely competitive. Acceptance rates are low, with only the highest ranked papers with solid experimental evidence being accepted. Because the fields are fast moving, conference publications are important for rapid dissemination of results. For Dr. Gerstlauer's fields, the top-tier conferences that are peer-reviewed and serve as a final publication venue include

- *IEEE Design Automation Conference*
- *IEEE Design, Automation and Test in Europe*
- *IEEE International Conference on Computer-Aided Design*
- *IEEE Symposium on Computer Arithmetic*

In rank, Dr. Gerstlauer has published 7 papers in top-tier conferences in addition to 9 journal papers.

In his research fields, Dr. Gerstlauer has published extensively in rank in top-tier journals (IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems; IEEE Trans. on Computers; and ACM Trans. on Design Automation of Electronic Systems) and top-tier conferences (IEEE Design, Automation & Test in Europe; IEEE Integrated Circuit Computer-Aided Design; IEEE Hardware/Software Co-Design and System Synthesis; IEEE Symposium on Computer Arithmetic). IEEE is the primary international technical organization for electrical and computer engineers, as ACM is for computer scientists.

Dr. Gerstlauer has collaborated and published with ECE and CS faculty at UT Austin, which is highly encouraged by our BC. As is the norm in his area, Dr. Gerstlauer works closely with his students, and much of his work is co-authored with them. His PhD student, Ardavan Pedram, won the Best Poster Award in the PhD Forum at the 2013 International Parallel and Distributed Processing Symposium.

Impact

Dr. Gerstlauer's work has had a significant impact on his field. His papers are very well cited. According to Google scholar, he has six papers with over 60 citations each:

- 645 for book *SpecC: Specification Language and Methodology* (2000)
- 177 for conference paper "RTOS Modeling for System-Level Design" (2003)
- 138 for book *System Design: A Practical Guide with SpecC* (2001)
- 120 for book *Embedded System Design: Modeling, Synthesis & Verification* (2009)
- 71 for journal paper "A SpecC-based framework for heterogeneous MPSoC design" (2008)
- 60 for journal paper "Electronic system-level synthesis methodologies" (2009)

The fourth and sixth publications were published while in rank at UT Austin. The second paper on the modeling of real-time operating systems (RTOS) received recognition in 2008 as one of the most influential papers in the previous ten years at the IEEE Design, Automation & Test in Europe Conference.

He co-authored the book *System Design: Modeling, Synthesis & Verification* (2009), which has been adopted at nine major universities in seven different countries. The hardcopy version sold 500+ copies, and chapters from the electronic version have been downloaded 4000+ times. He has been invited to publish and present five papers at the prestigious IEEE/ACM Asia and South Pacific Design Automation Conference in 2009, 2010 (x2), 2011 and 2012, as well as at two other international conferences.

His reference letters highlight his strong reputation and significance of his work. Below are examples:

> "I believe Dr. Gerstlauer is the key intellectual contributor behind the SpecC modeling language and methodology, which (besides the high citation counts) led to development of semantics for the SystemC language, which is now the default industry standard specification language for mixed hardware/software design implementations. The impact of this work is impressive, particularly coming from a researcher who is so early in his career." Prof. Nikhil Dutt, UC Irvine
>
> "There is a good balance between tools versus design papers. For me Andreas work would lack credibility without the design papers. The topics covered by these papers are of central concern in ESL. I also found the architecture modeling paper and the OS paper together offering some creative insights in a difficult modeling question." Prof. Arvind, MIT
>
> "It is also remarkable that the initial success he had as a PhD student seemlessly transformed into research success when starting to work independently as an Assistant Professor at UT Austin." Prof. Joerg Henkel, Karlsruhe Institute of Technology
>
> "I believe that his work is of exceptional quality and rigor, and the type of work that those of us who have to bridge between academia and commercial practice look for. Dr. Gerstlauer achieves this rigor and detail without sacrificing his quest for the fundamentals of elegance and abstraction, thus allowing his work to be simultaneously of academic and practical importance." Dr. H. Peter Hofstee, IBM Austin Research Laboratory
>
> "I think that Andreas is a rising star. He has come out of the research group of a prominent thesis advisor and has established himself as a strong technical leader in the computer system design methodology field. His research group's software is being used and is influencing other research. I enthusiastically endorse his promotion to Associate Professor with tenure." Prof. Don Thomas, CMU
>
> "Andreas has an outstanding research, teaching and service record, and we would be glad to have him on our faculty here at UIUC. I strongly support his promotion.... Since joining UT Austin, Andreas has established a diverse and high-quality research program that is certainly on par with if not better than any of his peers." Prof. Martin Wong, University of Illinois, Urbana-Champaign

Research Funding Generated

Dr. Gerstlauer has received significant external research funding, as shown in the table below. He has been awarded 12 funded research projects totaling $2.18M, with his share being $1.3M. He was Principal Investigator (PI) on both competitive National Science Foundation (NSF) grants and both competitive

Semiconductor Research Corporation (SRC) contracts. He was co-PI on a joint contract with the Defense Advanced Research Projects Agency and Army Research Office, and sole PI on contracts with National Instruments (NI) and Samsung. He has complemented this funding with unrestricted research gifts from Intel, NI and Qualcomm as sole PI. Another positive aspect is that he has collaborated with several faculty members at UT Austin on generating research ideas and landing funding for them: Profs. Heath (ECE), John (ECE), Orshansky (ECE), Pingali (Computer Science) and van de Geijn (Computer Science).

Source	Type	Total	Gerstlauer's Share
NSF (PI)	Grant	$ 450K	$ 225K
NSF (PI)	Grant	$ 500K	$ 250K
SRC (PI)	Contract	$ 255K	$ 255K
SRC (PI)	Contract	$ 345K	$ 173K
DARPA/Army Res. Office (co-PI)	Contract	$ 200K	$ 100K
National Instruments (PI)	Contract	$ 60K	$ 60K
Samsung (PI)	Contract	$ 150K	$ 150K
NI, Qualcomm, Intel (PI)	Gift funding	$ 166K	$ 126K

About 80% of the ECE faculty members who have received tenure and promotion since 1984 have received a young investigator award from a US federal agency, such as the National Science Foundation CAREER Award. Although Dr. Gerstlauer has not yet won a young investigator award, he has demonstrated success in landing funding on three competitive proposals from US federal agencies—two from the National Science Foundation as PI and one from DARPA/ARO as co-PI. Most important, Dr. Gerstlauer has developed sustained funding from a diversity of funding sources that is in excess of what is needed to sustain a research group in his fields of embedded systems and electronic design automation.

Peer Comparison

The following table represents a peer comparison. After receiving a PhD degree in 2004 from UC Irvine and working an Assistant Researcher at UC Irvine from 2004 to 2008, Dr. Gerstlauer joined the faculty at UT Austin in fall 2008 as an Assistant Professor. All of the other faculty members listed in the table below are Associate Professors. The table shows the dates of their hiring as faculty members and promotion to Associate Professor, as well as the numbers of conference papers, top-tier conference papers and journal papers published at the time of their promotion to Associate Professor. The top-tier conferences, as mentioned earlier in the Publications section, serve as terminal peer-reviewed publication venues in an way that is equivalent to peer-reviewed journal papers. An H-index attempts to measure productivity and impact of published work. An H-index of 21 means that the author has 21 publications with each paper having at least 21 citations and no other publication has more than 21 citations. The H-index values below were computed in August 2013 for all publications of each faculty member.

Faculty Member	Institution	Hired	Tenure	Conf. Pubs	Trans. Pubs	Students	Area	H-Index
Valeria Bertacco	Michigan	2003	2009	29	10	10	CAD	24
Luca Carloni	Columbia	2004	2009	26	5	10	Embedded	29
Andreas Gerstlauer	**UT Austin**	**2008**		**32**	**7**	**9**	**Embedded and CAD**	**21**
Vincent Mooney	Georgia Tech	1998	2004	33	6	8	Embedded	23
Sanjit Seshia	UC Berkeley	2005	2011	26	8	4	Embedded	23
T. Simunic-Rosing	UC San Diego	2005	2010	35	9	8	Embedded	29

In all measures given above, Dr. Gerstlauer compares favorably with his peers. His H-index of 21 is quite high for someone being considered for promotion to Associate Professor, as mentioned explicitly by one of the external letter writers:

> "The impact of his research can also be quantified… an H-Index of 21, which is excellent given that he is currently at a stage of his career where is considered to be promoted the rank of Associate Professor with Tenure…" Prof. Joerg Henkel, Karlsruhe Institute of Technology

Summary

In summary, the ECE Budget Council believes that Dr. Gerstlauer's research track record is outstanding. His letters of reference similarly articulate the view that his research is of the highest quality, and his productivity is comparable to the top researchers at the same point in their careers.

Prepared by Electrical and Computer Engineering Budget Council Members

Jacob Abraham Brian L. Evans Yale N. Patt

FIVE SIGNIFICANT WORKS

All references to publications are indexed on the resume, where [Jxx] is used to indicate journal articles, [Cxx] conference papers, [Pxx] book chapters, and [Bxx] books.

List of five most significant publications while in rank

J5. A. Gerstlauer, C. Haubelt, A. D. Pimentel, T. P. Stefanov, D. D. Gajski, J. Teich, "Electronic System-Level Synthesis Methodologies," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 28, no. 10, pp. 1517-1530, October 2009.

J6. G. Schirner, A. Gerstlauer, R. Dömer, "Fast and Accurate Processor Models for Efficient MPSoC Design," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 15, no. 2, article no. 10, pp. 1-26, February 2010.

J8. P. Razaghi, A. Gerstlauer, "Predictive OS Modeling for Host-Compiled Simulation of Periodic Real-Time Task Sets," *IEEE Embedded System Letters*, vol. 4, no. 1, pp. 5-8, March 2012.

J9. A. Pedram, R. A. van de Geijn, A. Gerstlauer, "Codesign Tradeoffs for High-Performance, Low-Power Linear Algebra Architectures," *IEEE Transactions on Computers (TC)*, special issue on Energy Efficient Computing, vol. 61, no. 12, pp. 1724-1736, December 2012.

J11. K. He, A. Gerstlauer, M. Orshansky, "Circuit-Level Timing-Error Acceptance for Design of Energy-Efficient DCT/IDCT-based Systems," *IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)*, vol. 23, no. 6, pp. 961-974, June 2013.

ANDREAS GERSTLAUER
Statement on Research

My research is broadly concerned with system-level design of embedded computer systems, where a specific focus has been on system-level design automation methodologies, technologies, and tools. During my time as a Ph.D. student and research faculty, I did fundamental, standard-setting work on system-level modeling, design languages and design methodologies. As a professor, I now lead a research group in the realization of automated design flows for synthesis of high-level system specifications into multi-processor and multi-core system-on-chip (MPCSoC) architectures that consist of heterogeneous hardware and software components.

A special emphasis has been on emerging design challenges at the boundaries of embedded and general-purpose computing. Embedded systems have traditionally been the domain of application-specific design. However, with rising chip design costs and power, thermal and reliability concerns driving competing needs for flexibility and specialization, I see traditionally separate areas merging. Future systems in both domains are expected to integrate tens to hundreds of diverse cores on a chip. Associated complexity and heterogeneity concerns make traditional design approaches infeasible. Consequently, my research interests have been focused on novel concepts and techniques for modeling, design, and implementation of such systems. This is aimed at reducing design cycles, exposing fundamental design tradeoffs, performing novel optimizations, and thus enabling whole new classes of high-performance yet tightly constrained desktop, server, mobile, and deeply embedded systems to be developed. System-level design automation approaches can thereby provide solutions that can aid both in automated exploration of the design space as well as in automatic compilation of high-level, parallel application programming models onto heterogeneous system platforms of the future.

My work has impacted system-level design practice and research in both academia and industry. I am co-author of 3 books and have published over 60 papers, a majority of which have been presented in top-ranked journals (IEEE/ACM Transactions) and high-quality international IEEE/ACM conferences (serving as terminal publication points for the best work in the field and having acceptance rates in the 17%-34% range). One of these papers was awarded as one of the best papers in the last 10 years at the Design, Automation and Test in Europe (DATE) conference, which is one of the top two conferences in the field. In addition to receiving more than 2100 total citations with an h-index of 21 (based on Google Scholar data), I have presented my work in various conference and industry tutorials, as well as more than 40 keynotes and invited talks in industry and academia. Furthermore, tools developed in my group are in active use for research and teaching at several universities worldwide. My work has also found adoption in industry. Tools have been evaluated and licensed by several partners such as Xilinx or Intel, and commercial derivatives are in use at the Japanese Aerospace Exploration Agency, NEC Toshiba Space Systems and others.

I have a well funded and well balanced research program. My funding totals more than $2M, with my share exceeding $1.3M. My research has been supported by competitive fundamental research grants from the US National Science Foundation (NSF), competitive applied research grants from the Semiconductor Research Corporation (SRC), and direct funding from AMD, Intel, National Instruments, Qualcomm and Samsung. Since coming to UT Austin, I have been specifically interested in initiating new interdisciplinary research thrusts. This has led to several successful NSF and SRC proposals on which I am the PI together with a team of collaborators in Electrical and Computer Engineering and Computer Science. My research program is also different from many of my peers in that I strive to maintain and establish tight collaborations with industry. These relationships have led to contract and gift funding as well as technology transfer in the form of opportunities for my students or licensing of research results.

Specific projects and contributions of my research lie in the areas of: (1) heterogeneous MPCSoC modeling, (2) system compilation and synthesis, and (3) design of novel energy-efficient system components and architectures. In the following, I describe my contributions in these areas in more detail. All citations refer to the publication list in my CV.

SYSTEM MODELING

At the core of any automated design process are well-defined models that provide abstract representations of a design at various stages. Models allow designers or tools to reason about optimization alternatives, to evaluate candidate designs before they are built, and to gradually refine a chosen design down to a final implementation. During my Ph.D. and post-doctoral time, I originally

developed and defined a comprehensive set of system models for automatic, stepwise exploration, validation and synthesis. Results have been published in several papers [C2-C12, J1-J2] and three books [B1, B3, B7], which have been translated into other languages [B2, B4, B5] and have received more than 850 citations combined. I am first author on [B3] with more than 130 citations. Back then, the focus in academia was also on developing standardized system-level design languages (SLDLs) for capturing such models. Driving language development from methodology and modeling requirements, I continue to be part of the project defining the SpecC language [C7, D1, and D2]. SpecC has been cited as a major reference for the development of SystemC, and these languages are industry standards for modeling of embedded systems and systems-on-chip (SoCs) today.

Simulation Backplanes Languages alone only provide a basic infrastructure on top of which actual modeling and automation concepts need to be developed. For systems with complex dynamic behavior, simulations remain one of the primary mechanisms for early validation and virtual prototyping. With ever increasing complexities, there is an urgent need for fast yet accurate simulators. Faster simulation can principally be achieved in two ways: (a) accelerating the simulation on the underlying host machine or (b) finding better abstractions to reduce simulation overhead. In my research, I have been interested in both. In collaborations with the original SpecC inventors at UC Irvine and colleagues at UT Austin, I have investigated fundamental approaches for parallelization of SLDL simulation kernels [C29] and cyber-physical co-simulation backplanes [C36, C47, J12]. This has resulted in general simulator frameworks that can achieve significant speedups on parallel and distributed hosts.

The main research focus in my group at present is on novel modeling abstractions. Traditional system simulators are either inaccurate or slow. On the communication side, transaction-level models (TLMs) have become a popular vehicle for abstract modeling of component interactions. I originally defined and analyzed one of the first applications of TLMs for system modeling at various levels of abstraction [C12, J2]. However, back then, similar approaches for fast yet accurate simulation of computation executing on processors were lacking. Research in my group is aimed at filling this gap. I was among the first to identify and propose a holistic approach for fast and accurate simulation of complete SoCs, for which I introduced the term *host-compiled modeling* in the invited papers [C26, C27, C38].

Host-Compiled Modeling In traditional discrete simulators, the granularity and detail of the simulated model determines a fundamental tradeoff between accuracy and speed. To overcome this tradeoff, the idea is to statically abstract as much implementation detail as possible while only simulating the dynamic aspects of a system that can not be accurately estimated otherwise. The difficulty lies in finding the right abstractions. In host-compiled models, speed is achieved by directly and natively executing dynamic application functionality on the host. For accuracy, the code then needs to be further back-annotated with appropriately estimated metrics, such as execution delays. Finally, code has to be simulated on top of very fast and lightweight yet accurate simulation models of operating systems (OSs) and processors, which in turn integrate into standard backplanes for co-simulation of complete multi-processor systems.

I have contributed in all of these aspects. My research in this area dates back to original papers on source-level profiling [C10, C11] and abstract OS modeling [C8]. The latter has received more than 170 citations, and it has been reprinted as a significant contribution to the field in [P2] and, in 2008, as one of the most influential papers in 10 years at DATE [P3]. In continued collaboration with former colleagues and co-advised students at UC Irvine (now faculty at Northeastern University), we extended these approaches to create one of the first high-level models of complete processors [C17, J6]. Within this context, I and my students at UT Austin were also the first to introduce the idea of host-compiled cache modeling [C24, C48], which has just recently begun to spawn similar research by others.

At UT Austin, I have worked with my students on expanding the scope, accuracy, and speed of host-compiled models. With my M.S./Ph.D. students Suhas Chakravarty and Zhuoran Zhao, I have built an infrastructure for optimized estimation and back-annotation of timing and energy metrics such that close to source-level simulation speeds of 1500MIPS at more than 99% accuracy can be achieved [C52]. In projects funded by SRC and in collaboration with partners at Freescale and Texas Instruments, we are currently extending models towards capturing a full range of performance, energy, reliability, power. and thermal metrics, as well as techniques for automatic calibration against existing low-level descriptions.

With recent trends towards increasing use of multi-core and multi-processor platforms even in the embedded space, I have worked with my Ph.D. student Parisa Razaghi on extending existing OS and processor models to capture real-time effects on such platforms [C31]. With a lack of analytical models in this domain, there is a need for fast and accurate simulators. Moreover, we have been able to show that even in slow, fine-grained simulations, errors can potentially become unbounded. This is a serious

concern in real-time system evaluation. The corresponding analysis was published in [J8], which was among the top-5 downloaded IEEE Embedded System Letters papers in April, August and November 2012. We subsequently proposed a solution in which the OS model dynamically and adaptively controls the granularity of the simulation to completely avoid such errors [C37]. With this, full-system simulations at the speed of a coarse-grain model but with fine-grain accuracy are possible. We are currently extending this approach to incorporate interactions with other components and shared caches equally managed by the OS model. Parisa is expected to defend her dissertation on this work in Fall 2013.

SYSTEM SYNTHESIS AND COMPILATION

Well-defined models are the basis for subsequent automation of the design process. This includes fast and accurate models for feedback and evaluation as well as formal models for specification of desired behavior. In collaborations with research groups at the Universities of Amsterdam and Leiden, Netherlands and the University of Erlangen-Nuremberg, Germany, I identified necessary ingredients and models for system design. A resulting novel taxonomy for classification of system-level synthesis approaches was published in [J5], which has already received more than 50 citations since 2010. In general, synthesis and exploration are iterative processes of making design decisions, generating a refined model that reflects those decisions, and evaluating this model to determine design quality and subsequently refine decisions under a set of optimization criteria and constraints. Building on host-compiled models for evaluation, I have been researching solutions for automating the decision making and model refinement processes. This is aimed at establishing a complete *system compiler* that can automatically and optimally map parallel application models onto heterogeneous MPCSoC platforms.

Model Generation Traditionally, system models are manually written, which is a tedious, error-prone, and time-consuming process. To supersede the need for dealing with coding details, I originally developed concepts and tools for automatic generation of models given a set of design decisions in my Ph.D. and post-doc work [C13-C15, J2]. Such tools have been integrated under a common graphical user interface in the System-On-Chip Design Environment (SCE) [J4]. I was one of the major contributors and project lead for implementation of the SCE tool set and its commercial derivative [C21]. SCE is aimed at realizing a user-driven, interactive, and automated system compiler. In ongoing collaborations with UC Irvine and Northeastern University, many of my research results continue to flow into the development of SCE.

A specific emphasis in my research has been on support for backend synthesis of actual hardware and software implementations. A key concern is the translation of high-level inter-processor communication into optimized hardware/software implementations that realize necessary interactions across a complex MPCSoC platform. On the software side, automatically generated, target-specific application code and device drivers are integrated into an off-the-shelf or custom-generated OS to synthesize final binary executables for each processor [C19, C20, C25]. On the hardware side, custom [C18, J3] or off-the-shelf synthesis tools are combined with automatic generation of area- and latency-optimized bus interfaces [C42]. Combined, this establishes a complete flow for compilation of generic parallel programming models down to heterogeneous hardware/software platforms.

Mapping and Scheduling To realize a complete synthesis solution, a system compiler can be integrated with algorithms for automated decision making and design space exploration (DSE). In case of system synthesis, this includes decisions about optimized partitioning and scheduling of parallel applications on heterogeneous MPCSoC architectures. In [J5], I and my collaborators surveyed the system-level synthesis landscape using the taxonomy we derived. Based on insights from this study, we have developed some of the first complete synthesis solutions by coupling existing DSE tools from my collaborators with the model generation and implementation synthesis backend in SCE [C28, J7].

Leveraging fast and accurate host-compiled simulation models within generic optimization engines (such as genetic algorithms) enables rapid exploration. By contrast, in restricted application domains, such as image, video or signal processing, simulations can be completely replaced by static analysis. However, inherently intractable complexity of corresponding optimization problems limits achievable results. In collaborations with National Instruments (NI) and students of my colleague Brian Evans, I have developed novel heuristics that combine genetic optimizers with integer linear programming (ILP) formulations to jointly optimize throughput and latency while considering both computation and communication [C32, J10]. By applying a two-stage approach, we are able to achieve near-optimal results in low runtime. In continued collaboration with NI and my students, I am currently investigating further improved heuristics for heterogeneous mapping, partitioning, and scheduling.

ENERGY-EFFICIENT SYSTEMS

Energy efficiency is arguably one of the primary concerns in both embedded and general purpose computing. Beyond power-aware modeling and synthesis, I have, since coming to UT Austin, established new research initiatives and collaborations to investigate hardware/software foundations for the design of highly energy-efficient computer systems. Fundamentally, energy efficiency can be achieved in two ways: (a) reducing the amount of overhead per computation or (b) reducing the amount of computation itself. I am PI on NSF-funded collaborative projects that have contributed in both aspects.

Algorithm/Architecture Co-Design of Domain-Specific Processors With semiconductor technology scaling reaching physical limits, it is predicted that power and cooling concerns will limit the active area of a chip to only around 10-50% at any given time (dark silicon). At the same time, it is well-accepted that reducing overhead through specialization can achieve order of magnitude gains in both performance and power consumption. As such, future chips can and must have specialized cores that are turned on only when needed. However, full-custom design is also becoming prohibitively expensive. The key questions are therefore: what is the right mix of cores and what are the tradeoffs between specialization, achievable efficiency, and enough flexibility to implement a broad class of operations?

In collaboration with domain experts in the Computer Science Department at UT Austin, I am aiming to answer these questions for the domain of dense linear algebra applications, which are an important class of kernels both in high-performance and embedded computing. By co-designing algorithms and architectures for a dedicated Linear Algebra Processor (LAP), we have shown that it should be possible to achieve orders of magnitude better efficiencies compared to current architectures [C33, J9]. A prototypical LAP in 45nm is expected to maintain 600 GFLOPS in less than 25W with enough flexibility to support the full range of basic linear algebra subroutines (BLAS) [C40, C41]. We have also demonstrated that with minimal modifications of the architecture, the LAP can support many other operations, such as matrix factorizations [C46] or Fast Fourier Transforms (FFTs) with similar efficiencies [C49].

For his work on developing the LAP, the co-advised student on the project, Ardavan Pedram, has received the IEEE Computer Society Technical Committee on Parallel Processing (TCPP) Best Poster Award at the Ph.D. forum of the 2013 IEEE International Parallel & Distributed Processing Symposium (IPDPS). He is graduating in Summer 2013 and will continue on the project as a post-doc. We are currently investigating collaborations with companies, such as AMD and IBM, and other universities, such as Stanford University and the University of Wisconsin-Madison on integrating the LAP into other systems as well as LAP implementation and prototyping. Furthermore, in newly established projects with another student, I have started to apply such algorithm/architecture co-design concepts to applications in computational biology, where we are designing low-cost, yet high-performance processors and associated compilers for accelerated stochastic simulation of biochemical reaction networks [C50].

Approximate Computing Maintaining the notion that a computer always produces a perfect result is often unnecessarily expensive. Towards the goal of energy savings through reduced, i.e. approximated computations, I am, together with my colleague Michael Orshansky, investigating techniques for the design of hardware in application domains, such as digital signal processing, where inherent notions of signal quality allow for small reductions in output quality to be traded off for significant energy gains. There have been a range of approaches to exploit this inherent error tolerance. Recognizing that at the circuit level, traditional worst-case operation is suboptimal from an energy point of view, we have developed novel strategies for controlled acceptance of timing errors under aggressively reduced supply voltages. Naïve voltage overscaling in unmodified circuits leads to immediate and large errors. By instead exploiting algorithm, hardware, and input characteristics to minimize error probability and magnitude, and by applying novel low-energy post-processing techniques, we have been able to show that up to 50% energy savings are possible while maintaining a good output quality in typical image, video, and audio processing kernels, such as (I)DCTs [C30, J11] and digital filters [C45].

Voltage overscaling can have issues with circuit stability and verification. An alternative is to directly modify the Boolean logic of a circuit in order to produce an approximated output at reduced complexity and hence energy. In [C44], we have systematically investigated quality-energy optimal structures for basic arithmetic building blocks, such as adders and multipliers. In contrast to existing ad-hoc designs, we have shown the existence of a whole family of Pareto-optimal designs across the energy and quality space. We are currently generalizing this approach to develop algorithms for synthesis of general approximate circuits under arbitrary error magnitude and frequency constraints [C54]. The long-term goal is to integrate quality-energy optimizations into general hardware synthesis flows, algorithms and tools.

REFERENCES

All references to publications are indexed on the resume, where [Jxx] is used to indicate journal articles, [Cxx] conference papers, [Pxx] book chapters, and [Bxx] books.

List of five most significant publications while in rank

J5. A. Gerstlauer, C. Haubelt, A. D. Pimentel, T. P. Stefanov, D. D. Gajski, J. Teich, "Electronic System-Level Synthesis Methodologies," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 28, no. 10, pp. 1517-1530, October 2009.

J6. G. Schirner, A. Gerstlauer, R. Dömer, "Fast and Accurate Processor Models for Efficient MPSoC Design," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 15, no. 2, article no. 10, pp. 1-26, February 2010.

J8. P. Razaghi, A. Gerstlauer, "Predictive OS Modeling for Host-Compiled Simulation of Periodic Real-Time Task Sets," *IEEE Embedded System Letters*, vol. 4, no. 1, pp. 5-8, March 2012.

J9. A. Pedram, R. A. van de Geijn, A. Gerstlauer, "Codesign Tradeoffs for High-Performance, Low-Power Linear Algebra Architectures," *IEEE Transactions on Computers (TC)*, special issue on Energy Efficient Computing, vol. 61, no. 12, pp. 1724-1736, December 2012.

J11. K. He, A. Gerstlauer, M. Orshansky, "Circuit-Level Timing-Error Acceptance for Design of Energy-Efficient DCT/IDCT-based Systems," *IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)*, vol. 23, no. 6, pp. 961-974, June 2013.

SUMMARY OF RESEARCH OUTPUT

Publications (published and accepted)

Publication Type	In Rank	Total
Journal Articles	9	12
Conference Papers	32	54
Corresponding Author	4 (3 invited)	9 (4 invited)
Technical Reports	7	40
Book Chapters	2	5
Books	1	3
Citations*	1085	2108
h-Index*	17	21

* Per Google Scholar, 7/14/2013

Research Funding Raised

	In Rank		Career	
Funding Type	Total	My Share	Total	My Share
Contracts and Grants	$1.98M	$1.23M	$3.37M	$1.93M
Gifts	$0.19M	$0.15M	$0.19M	$0.15M
Total	$2.17M	$1.39M	$3.56M	$2.08M

Research Funding Received

	In Rank		Career	
Funding Type	Total	As PI	Total	As PI
Contracts and Grants	9	7	10	7
Gifts	4	3	4	3
Total	13	10	14	10

Grants and Contracts Awarded while in Rank

Co-Investigators	Title	Agency	Project Total	Candidate Share	Grant Period
-	Core Technology Development for System Simulation including Network	Samsung, Korea	$149,020	$149,020	6/1/2013-12/31/2013
-	Automated Design Space Exploration and Optimization of DSP Systems	National Instruments	$60,000	$60,000	8/1/2012-7/31/2013
Robert Heath (PI, ECE)	Interference Alignment in Distributed Environments	Army (ARO)	$99,980	$49,990	9/1/2012-8/31/2013
Lizy John, (Co-PI, ECE)	Multi-dimensional Modeling, Design and Exploration of Heterogeneous Multicore SoCs	SRC	$345,000	$173,000	8/1/2012–7/31/2015
Robert Heath (PI, ECE)	Interference Alignment in Distributed Environments	DARPA	$99,344	$49,672	9/1/2011-8/31/2012
-	Towards Enabling Full-Cell Biochemical Network Simulations	UT Austin, SRA	$20,000		7/1/2011-8/31/2011
Robert van de Geijn (Co-PI, CS)	SHF: Small: Algorithm/Architecture Co-Design of Low Power and High Performance Linear Algebra Compute Fabrics	NSF	$499,919	$249,959	6/1/2012-5/31/2015
Michael Orshansky (Co-PI, ECE)	SHF: Small: Formal Synthesis of Low-Energy Signal Processing Systems Relying on Controlled Timing-Error Acceptance	NSF	$449,614	$224,807	9/1/2010-8/31/2013
-	Automatic Platform Model Calibration and Tuning	SRC	$254,337	$254,337	8/1/2010-7/31/2013
			$1,977,214	$1,230,785	

Budget Council Assessment on Academic Advising, Counseling and other Student Services for Dr. Andreas Gerstlauer

This statement on the academic advising, counseling and other student services for Assistant Professor Andreas Gerstlauer was prepared by Professor David Z. Pan on behalf of the Budget Council. The statement was prepared following a review of his annual reports, and an in-depth knowledge of ECE departmental activities.

Academic Advising and Counseling

Dr. Gerstlauer has actively mentored and advised undergraduate students from freshmen to senior levels. He teaches a freshmen-level class (EE319), and encourages them to be part of the broader teaching and research community from the beginning of their college life. Several students of his EE319 later became undergraduate teaching assistants for EE319. He has represented the Integrated Circuits and Systems (ICS) area twice and given talks at the Tech Core Night, which is organized by the HKN honor society to help sophomore/junior-level students pick their tech areas and courses. He also presented his research to the undergraduate Research Seminar series (EE155R) and joined the informal HKN "fireside" chats to provide general student counseling. He has mentored two senior design teams comprised of five students each (EE464). He has also served as the Faculty Advisor to several upper-division undergraduate students in Computer Engineering (CE) and Embedded Systems tracks.

He actively participates in graduate student admission, recruitment, and retention activities. He is active in graduate admissions in three academic areas: Computer Architecture and Embedded Processor (CAEP), CE, and ICS. Altogether, these areas attract about one thousand applicants each year. Thus, the workload for reviewing their files, arranging the site visits, phone/Skype interviews, and so on, is huge. In a typical year, he may review over 150 students' application packages. As the ICS graduate admission coordinator, I have worked with Dr. Gerstlauer since he joined UT, and he is always a very reliable committee member who I can trust for the timeliness and quality of the tasks assigned to him.

He is also a co-organizer of the active ICS seminar series, encouraging and facilitating student participation in interactions with a steady stream of visitors, which helps to enrich graduate student's experiences at ICS.

Dr. Gerstlauer has a consistent record with all levels of undergraduate and graduate students. His careful advising has resulted in high quality students, student leaders, projects and publications.

Individual Student Supervision

Dr. Gerstlauer was the PhD co-supervisor of following three students who have obtained their PhD degrees.

- Ahmed Abdel Hadi (co-supervised by Prof. Sriram Vishwanath): PhD in December 2011. Currently a post-doc researcher at Virginia Tech
- Ku He (co-supervised by Prof. Michael Orshansky): PhD in May 2012. Currently a Digital Design Engineer at Cirrus Logic
- Ardavan Pedram (co-supervised by Prof. Robert van de Geijn at UTCS): PhD in August 2013. Currently a post-doc researcher at UT Austin

In addition, Dr. Gerstlauer has supervised three MS theses and five MS reports. He has served on the PhD dissertation committees of 10 students and the PhD qualifying examination committees of 22 students, which is quite above average for his duration at UT.

Currently, he is supervising or co-supervising a group of seven PhD students and two MS/PhD students. Three PhD students have advanced to candidacy, and two of them are expected to defend their PhD theses in Fall 2013, including Parisa Razaghi, to whom Dr. Gerstlauer is the sole supervisor.

In summary, in the areas of academic advising, counseling, and other student services, Dr. Gerstlauer's performance has been excellent, and he has consistently met our department's expectations for his rank.

Summary prepared by Budget Council Member Professor David Z. Pan.

David Z. Pan
Professor
Department of Electrical and Computer Engineering

ANDREAS GERSTLAUER
Statement on Academic Advising

Next to classroom teaching and individual supervision on research or other projects, I enjoy advising students at both the undergraduate and graduate level in the broader view of my field. In addition to the students in my own research group, I have advised many graduate students in the context of Research Problems courses, I regularly participate in undergraduate and graduate advising and recruiting events, I serve as faculty mentor for many students in our undergraduate embedded systems track, and I generally aim to provide broad guidance to students I interact with through my regular teaching activities. In all cases, I strive to strike a balance between moderating an environment in which students can mentor each other and giving out specific advice that is tailored to the individual needs and style of each student.

UNDERGRADUATE ADVISING

At the undergraduate level, I have actively participated in advising students both generally within my area as well as in personal interactions with individuals or student groups. Thus far, I have represented the Integrated Circuits and Systems (ICS) area in the Tech Core Night organized by the ECE Department's Eta Kappa Nu (HKN) honor society twice. In this event, lower-division students get exposed and oriented on the different technical areas offered as tracks for specialization in our undergraduate curriculum. This includes presentations by representatives from each area on course selections and career opportunities, which are followed by discussion and detailed question & answer sessions. In addition to these more organized events, I have also participated in HKN's so-called "fireside" chats in which students can ask questions and discuss any topic of their choice in a more informal setting. Finally, I have also presented my work in the undergraduate Research Seminar series (EE155R), which the ECE Department offers to upper-division students interested in further specialization and eventual graduate careers.

In general, I encourage all interested undergraduate students to become an active part of the broader teaching and research community. Several of the students who took my freshmen class have subsequently served as undergraduate teaching assistants for the same class. Furthermore, students in my classes have regularly approached me to ask for advice on selection of courses, choice of major or general career goals, such as plans and reasons for joining graduate school. I often incorporate corresponding discussions into my undergraduate lectures. Especially at the Freshmen level, I see it as important to expose students early on to the various opportunities and options available to them, stressing the importance of obtaining a graduate degree especially in such complex fields as computer engineering or very large-scale integrated circuits.

Apart from my interactions with individual students through lower-division teaching activities, I have also served as the official Faculty Advisor for several upper-division undergraduate students in the computer engineering and embedded systems tracks. After choosing their technical core, every student in the ECE Department is assigned a faculty advisor in his or her area. As a mentor, I meet with students to discuss aforementioned issues: selection of courses, electives and technical cores in alignment with long-term career goals of joining industry or graduate school. In the ECE Department, I also served as faculty mentor for two senior design teams with five students each. Apart from interfacing with students and industrial sponsors on the technical and management aspects, I use these project settings to be similarly available for students and to provide advice on a wider range of issues that are especially critical for seniors in their last year in college before entering the real world.

My interactions with students in undergraduate events, seminars, classes or projects regularly lead to students expressing interest in participating in research. While students in my Freshmen classes are often too early in their careers to be able to do meaningful work, I strive to maintain contact with such students throughout their time at UT in order to keep them interested in and aware of career opportunities in my group or elsewhere. Nevertheless, on some occasions I have had promising Freshmen become undergraduate research assistants. For example, after taking my class in Spring 2012, Kevin Gilbert joined my group for the summer of 2012, and he is now secretary for the IEEE Robotics and Automation Society at UT as well as a research assistant in another robotics group. Both he and Emily Ledbetter, another of the students I had in my class, have become active in various IEEE groups and have subsequently served as undergraduate TAs for the Freshmen class they previously took with me. They both enjoyed their experiences a lot and are motivated to pursue research and teaching careers. In addition, I have had several seniors enroll in one of my graduate classes, and I have actively supported graduate school applications for those and other students, such as members of my senior design teams.

GRADUATE ADVISING

At the graduate level, I participate in all areas of advising throughout a student's time at UT, including recruitment, retention, supervision, career placement and general advancement of personal and professional skills beyond just the degree. At the transition from undergraduate to graduate school, I am an active member of the Graduate Admission Committees of both the Computer Engineering/Computer Architecture and Embedded Processors (CE/CAEP) and the Integrated Circuits and Systems (ICS) tracks. In this capacity, I review more than 150 applications a year and I interface with prospective or admitted students via email or phone to help interview and recruit them. In addition, for the last four years I have served as the organizer of the site visit for prospective graduate students in the ICS track. We invite admitted students who are already in the US for a two-day visit in which we put together a program of talks, poster sessions and individual meetings to convince the most promising candidates to join UT. As the co-organizer, I am the main point of contact for visiting students in the ICS track. I also give overview presentations, arrange meetings with our students and faculty, and participate in various group and social events to more closely interact with students. Site visits are always very successful and we generally receive very positive feedback from visitors who leave with a strong impression about UT.

Being part of the admissions process allows me to actively recruit students at an early stage for my own group. Incoming students and students taking my introductory graduate classes during their first year at UT are the two main channels through which I recruit new members. At UT Austin, I have advised or co-advised 16 full-time graduate students so far. For one of these, Ahmed Abdel Hadi, I became co-supervisor after he had already started to work with Prof. Vishwanath. All other students have been recruited upon joining UT or shortly thereafter. Out of these 16, Ahmed and 2 other co-advised students have graduated with a Ph.D. and are now in post-doctoral or research-oriented positions in academia or industry. Furthermore, 4 students who graduated with M.S. degrees have joined large companies such as Intel or National Instruments. The remaining 9 students are currently still here at UT. I have also recruited a new student, Sabine Francis, to join my group in the Fall. Sabine decided to join UT rather than accept an offer for a Dean's Fellowship from Carnegie Mellon University (CMU). In addition to these full-time students, I have advised 3 part-time students from our professional masters program to the completion of their M.S. degrees. Furthermore, in 2009-2010 I hosted a visiting Ph.D. student as part of a collaboration between the ECE Departments at UT and at Monterrey Tech in Mexico. I subsequently became an external co-supervisor on her thesis. Martha successfully defended in May 2011 and has by now taken on a prestigious position as Director of a research program at another university in Monterrey.

In my group, I follow an advising style that combines discussions among the group with personal meetings with individual students or smaller groups. I hold irregular group meetings, usually in the context of dry-runs for student conference paper presentations. These group meetings are meant to expose students to other work going on in the group as well as allowing them to update others with their own progress in general terms. Due to the diverse nature of research in my group, I also hold weekly meetings with each student or with each group of students working on the same project. These meetings allow me to discuss research in detail, adjusting the general direction, if needed, and giving specific advice that is tuned to the needs and working style of each student. The goal is to find an approach, whether more hands-on or letting students work relatively autonomously, that recognizes that each student is different and that brings out the best in each. Crucially, advising styles may have to be adjusted as students mature and grow. Typically, new incoming students will require closer involvement while I expect students that have passed (or that want to pass) their candidacy exam to be able to work independently.

Part of the process of fostering student growth is to also advise students on soft and communication skills, such as time management and effective writing, speaking and presenting. I closely work with my students to continuously improve these aspects. Especially in engineering, I also deem it important that students understand the connection between their work and real-world problems and practices. I therefore actively help them to find internship opportunities. For example, with the exception of work restrictions on Iranian students, all my students are on internships at companies like Intel, Broadcom or National Instruments this summer. Internships or industry-sponsored research projects also often lead to job opportunities for students after their graduation. In general, I try to leverage my contacts within industry to help place students of mine who are interested in such careers. This specifically includes aligning such students with projects done in collaboration with companies. For students interested in academic careers, I try to exploit all opportunities to introduce them to other leading researchers in the field. I generally support all my students in attending top conferences, which I consider essential not only from a networking perspective but also to expose them to the latest developments in the area.

In addition to students in my own group, I help to advise other students by serving on their M.S. or Ph.D. committees, by collaborating with students supervised by other faculty, and by mentoring incoming graduate students that come to my office but do not have a dedicated supervisor yet. I also aim to generally contribute to a successful research culture in the department and in my area. For example, over several semesters I organized the seminar series of the Integrated Circuits and Systems Group (ICSG), and I continue to regularly invite speakers on a range of topics to give seminar talks here at UT. Some of the most exciting opportunities for future advances often lie at the intersection of traditionally disconnected areas. As with my own students, I therefore view being exposed to a broad range of ideas rather than just ones own narrow research topic to be instrumental in the personal and professional growth of future generations of leaders.

SUMMARY OF ACADEMIC ADVISING

Student Supervision

Student Type	In Rank (As Sole Advisor)	Total (As Sole Advisor)
Student Organizations Advised	2 (HKN Tech Area Nights)	
Undergraduates Supervised	1 (1)	
Senior Design Teams Mentored	2 (2)	
Ph.D. Graduated*	1.5 (0)	2.5 (0)
Ph.D. In Candidacy*	2 (1)	
Ph.D. In Progress*	4 (4)	
M.S. Graduated*	7.5 (7)	7.5 (7)
M.S. In Progress*	2 (2)	

* Counted as 1 if sole advisor, 0.5 if co-advised

Completed Graduate Students under My Supervision at UT Austin

Student	Co-Supervisor	Degree	Start	Thesis	Placement
Ardavan Pedram	Robert van de Geijn (CS)	Ph.D.	09/2007	08/2013	UT Austin*
Ku He	Michael Orshansky	Ph.D.	09/2007	05/2012	Cirrus Logic
Ahmed Abdel Hadi	Sriram Vishwanath	Ph.D.	09/2008	10/2011	Virginia Tech.*
Jin Miao	Michael Orshansky	M.S.	09/2010	12/2012	UT Austin†
Ashmita Sinha	-	M.S.	09/2010	08/2012	Intel
Manan Kathuria	-	M.S.	01/2009	05/2012	Intel
Arindam Goswami	-	M.S.	09/2009	08/2011	Nat'l. Instruments
Pablo S. Bomfim	-	M.S.	09/2008	05/2010	Startup, Paraguay

* Post-doctoral researcher, † Ph.D. student

A complete list of supervised students, students in progress, and service on M.S. and Ph.D. committees is provided in the Teaching Statement.

Budget Council Assessment on Service to the University and to the Nation, State, and Community for Promotion Candidate Andreas Gerstlauer

This statement on service to the University, the Nation, State, and Community by Professor Gerstlauer was prepared by Electrical and Computer Engineering Budget Council member, Jeffrey Andrews.

Prof. Gerstlauer has provided a great deal of service and leadership to his research community and the University of Texas, especially for someone at his career stage. I will now summarize these contributions and their importance.

Professional Service and Leadership

Prof. Gerstlauer has served in many visible and important research roles in his time as an Assistant Professor at UT Austin. In particular, he has held leadership positions at three prestigious conferences in his field. These include:

1. Chairing for the past two years the Electronic Design Automation 1 (EDA1) Track subcommittee at the top-tier *Design Automation Conference*. This is the premier conference in his research area, and EDA1 is the core track on "System-Level Design & Codesign"
2. Chairing the "Architecture and Implementation" Area at the 2013 Asilomar Conference on Signals, Systems, and Computers. This is a very high quality workshop near Monterey, CA with a rich history across many research areas.
3. Chairing the "Hardware/Software Co-Design" Track at the 2009 and 2010 International Conference on Hardware/Software Co-Design and System Synthesis (CODES+ISSS), which is the top conference in his core research area.

Prof. Gerstlauer has also participated in many other roles at many other conferences, both international as well as those hosted by UT Austin, that bring distinction and visibility to what is happening at our university. These are detailed in his Service Statement and CV.

Although conferences are the main top-tier publication venue in Andreas's research area of embedded systems and design automation, he also has found time to serve as an Associate Editor for the ACM Transactions on Embedded Computing Systems. As expected for an ACM Transactions, this is one of the premier journals on Embedded Computing. He is also one of the select few who is an Associate Editor for the Design Automation for Embedded Systems journal.

Combining both his conference and journal duties results in an unusually large quantity of top-tier service positions for a junior faculty member, and bodes well for

Andreas's future during which we expect to see him assume increasingly important IEEE and ACM leadership positions.

Service to the Department, College, and University

Prof. Gerstlauer has also been an excellent citizen in the department, contributing generously across multiple research and academic areas. For example, he serves on the admissions committees of both the Computer Engineering/Computer Architecture and Embedded Processors (CE/CAEP) track and the Integrated Circuits and Systems (ICS) track. This is very time-consuming and important work that does not show up on one's CV.

He is similarly involved in research units, including both CERC and WNCG. As the WNCG Director from 2008-2012, I can particularly speak to his involvement with WNCG. I approached him to join as several of our industrial affiliates were interested in the flexible implementation of wireless communication and networking algorithms. We had him present his work to a few of them, and they were very impressed. Since joining, he has become a core member of the group, which is a time-consuming and unselfish commitment to the center. His contributions have included visiting our affiliates in person many times to share his research with them, attending nearly all meetings (which are frequent), contributing to our internal needs, like reporting and meeting organization, and otherwise supporting the affiliates program. I know the affiliates consider him to be a valuable addition to the group.

To summarize, Prof. Gerstlauer has easily exceeded the expectations of service for promotion to Associate Professor. He has undeniable leadership qualities and potential, and we look forward to him growing into future leadership roles.

Summary prepared by Budget Council Member Jeffrey Andrews.

JG Andrews

ANDREAS GERSTLAUER
Statement on Service

Teaching, research and service are the three main pillars of the academic profession. In terms of service, I have been actively involved at the university, community and national level. At UT, I have participated in 7 departmental committees. I have served the broader professional community by being involved in the organization of 16 conferences and workshops, by serving on 25 technical program and 2 editorial committees, and by reviewing papers for more than 20 journals, conferences and workshops. Finally, I have also served on grant review panels for federal funding agencies. In the following, I will summarize and highlight my main service activities. A complete list of my service contributions is available in my CV.

SERVICE TO THE UNIVERSITY

I have been involved in the university as a member of several important departmental committees.

Faculty Searches In 2010, I was member of the Faculty Search Committee for an Assistant Professor position in the broad area of embedded systems. As a member of the committee, I helped review and select faculty applications, I interviewed promising applicants over the phone, and I served as the host organizing the on-site visit and interview of one invited candidate. In the end, we made an offer to Nan Sun, who subsequently accepted and is now a colleague in my department.

Graduate Admissions Ever since I joined the ECE Department in 2008, I have been deeply involved in the graduate admissions process. I am a member of the Graduate Admissions Committee of two tracks, the Computer Engineering/Computer Architecture and Embedded Processors (CE/CAEP) track and the Integrated Circuits and Systems (ICS) track. As part of these committees, I regularly review more than 150 applications and I help interview promising students over the phone. Furthermore, since Spring 2010 I have served as the coordinator of the prospective graduate student site visit for the ICS track. Within this role, I give overview presentations, I arrange meetings between students and faculty, I participate in group and social events, and I serve as the main contact point and host for visiting students.

Curriculum and Degree Committees As part of the ECE faculty, I am member of the department's Graduate Studies Committee (GSC), which determines curriculum and degree requirements for ECE graduate students. In addition, I am member of the Curriculum Committees of the CE/CAEP and ICS tracks at the undergraduate and graduate levels. Within these committees, we determine and propose the curriculum and degree requirements within each respective specialization. My participation in undergraduate curriculum development in the CE track is further detailed in my Teaching Statement.

Centers and Research Units I am an active member of two research centers at UT Austin, namely the Wireless Networking and Communications Group (WNCG) and the Computer Engineering Research Center (CERC). In this capacity, I am engaged in weekly center meetings and all aspects of running the organized research units (ORUs), including recruiting industrial affiliates, maintaining affiliate relationships, participating in and organizing yearly board meetings and open houses, student recruiting, space allocations, web page updates and general publicity.

SERVICE TO THE PROFESSIONAL COMMUNITY

I have been very active throughout the years in serving my broader academic community, which includes organizing conferences, serving on conference and journal committees, as well as reviewing papers.

Conference Organization I have served in various leadership roles for the organization of major international conferences as well as smaller, focused workshops in my area. For the past two years, I have been Chair of the EDA1 subcommittee at the Design Automation Conference (DAC), which is the premier conference in my field and regularly draws more than 1500 attendees for its technical sessions. I similarly served as Area Chair for the 2013 Asilomar Conference on Signals, Systems and Computers (ACSSC), where I handled the paper selection among 60 submissions. In 2009 and 2010, I also served as Track Chair for the International Conference on Hardware/Software Co-Design and System Synthesis (CODES+ISSS), which is the top conference in my area. In addition, I have been Track Co-Chair, Local Arrangements Chair, and Registration Chair for several other conferences. Furthermore, I have organized or co-organized special sessions on new research directions at major conferences such as DAC.

Apart from participation in the organization of larger conferences, I have also served as overall Program Chair, Co-Chair, or Organizer for several smaller, more specialized conferences and workshops. This included the Workshop on Compiler-Assisted System-On-Chip Assembly (CASA), which entirely consists of invited presentations by leading experts in the field. Furthermore, I was Tutorial Chair and Technical Program Committee Chair for the 2009 and 2010 Austin Conference on Integrated Systems and Circuits (ACISC), respectively. ACISC was an annual event organized by the Integrated Circuits and Systems Group (ICSG) at UT to promote the university in the local and state's semiconductor community. The 2010 conference included keynotes, invited talks and panels with more than 60 attendees.

Conference and Journal Committees My area is a conference-driven field, and I have served for several years on Technical Program Committees of many major international conferences, including DAC, CODES+ISSS, the International Conference on Computer Design (ICCD), and the Design, Automation and Test in Europe Conference (DATE) (the European counterpart to and a similarly premier event as DAC).

I also serve on Editorial Boards of journals. I am an Associate Editor for the ACM Transactions on Embedded Computing Systems (TECS) (which is one of the top journals in my field) and the Design Automation for Embedded Systems (DAES) journal by Springer (another specialized journal in my area that has many other leading experts in the embedded systems domain on its editorial board).

Conference and Journal Reviews Outside of direct involvement with conference or journal committees, I frequently accept invitations to serve as an external reviewer for top conferences and journals, including all the major ACM and IEEE journals in my field.

OTHER SERVICE

Within my department, I have for two semesters helped to organize the Integrated Circuits and Systems seminar series, which is a regular series of invited talks by leading experts in the broader semiconductor area attended both by students at UT as well as engineers and scientists from local industry. At the national level, I have served as reviewer of grant proposals on a panel organized by the National Science Foundation (NSF). Finally, internationally I have been invited to serve as an external expert reviewer/opponent on two Ph.D. dissertations at the University of Tübingen and the University of Paderborn in Germany in 2012 and 2010, respectively.

Budget Council Assessment on Honors and Other Evidence of Merit or Recognition for Tenure and Promotion Candidate Andreas Gerstlauer

This statement on honors and recognition for Prof. Andreas Gerstlauer was prepared by Electrical and Computer Engineering Budget Council member Lizy K. John. This statement was prepared based on the candidate's CV, his own statement of honors and my personal knowledge of his achievements. I have been on the Ph. D committee of one of his students who received a Best Poster award at an IEEE conference. I have also written several joint proposals with him. Relying on my personal knowledge and his CV, I make the following observations.

Dr. Gerstlauer's research is well recognized by his peer community. His papers have been cited more than 2000 times, according to Google Scholar. He has written 3 books, of which one was a top 10 technical book in Japan when it came out. Another book is in the top 25% of the most downloaded eBooks in its category from Springer in 2012.

He gave a keynote speech at the 2011 Brazilian Symposium on Computing System Engineering, an honor rarely found on an Assistant Professor's CV. He has also given various talks nationally and internationally (29 talks world-wide).

Dr. Gerstlauer's Ph. D student, Ardavan Pedram, won the award for the best poster at the IEEE International Parallel and Distributed Processing Symposium (IPDPS) in 2013. Another significant achievement was the selection of one of his papers by the Design, Automation and Test in Europe conference as one of the most influential papers in 10 years. While this paper was written before he came to UT, the selection happened after he came here and it brings honor and recognition to the university.

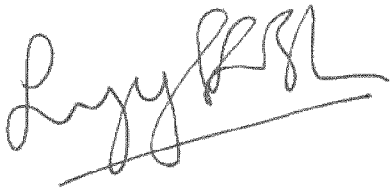
Dr. Gerstlauer received several competitive grant awards, also illustrating that his work is well regarded by his peers nationally and internationally. He has several competitive grants, two from National Science Foundation (a third one tentatively funded), two from the Semiconductor Research Consortium (SRC), one from Samsung Korea, and one from the Army Research Office. In addition, another NSF grant is tentatively approved, and a grant from Intel is also tentatively approved (I am a co-PI on both of these). Dr. Gerstlauer has a clearly demonstrated track

record of success in funding his research initiatives through both industrial and governmental means.

Dr. Gerstlauer is an associate editor for ACM Transactions on Embedded Computing Systems (TECS). He has been on the editorial board for Design Automation for Embedded Systems since 2012. These represent significant achievements, because usually such editorial committee contributions do not appear on Assistant Professor's CV. He has also served as reviewer for the National Science Foundation. In our field, being invited to serve on a conference technical program committee or review panel is an honor, because the committee chairs are recognizing the stature of the invitee. While in rank, he served as Chair or co-chair of 5 technical program committees and was a member of several, including the prestigious DAC conference. All of these indicate that he is regarded as a prominent international contributor to the field of embedded systems.

Prof. Gerstlauer's research is well recognized nationally and internationally, and he has received an extraordinary number of honors and meritorious recognitions, as evidenced above.

Summary prepared by Budget Council member Lizy K. John.



ANDREAS GERSTLAUER
Statement on Honors and Recognition

My work at UT Austin has been recognized by the community in a variety of ways. I have received competitive funding, my research has been selected and awarded for being among the best within a venue or the field, and I have been invited to speak at conferences, other universities and in industry. In the following, I will summarize my funding, honors, awards and other recognitions of merit I received. Further details are available in my resume. All citations refer to publications listed there, where [Jxx] indicates journal articles, [Cxx] conference papers, [Pxx] book chapters, and [Bxx] books.

FUNDING

My research at UT has been supported by a mix of funds from different sources, with about 65% of my share of funding coming from competitive grants (more than half of that or about 35% total in the form of National Science Foundation awards), about 20% through other industry or government contracts (8% total from the Department of Defense), and the remaining 10% as industry gifts. I am PI on four highly competitive grants from federal agencies and industry consortia, two each from the National Science Foundation (NSF) and the Semiconductor Research Corporation (SRC). I am sole PI on the SRC grant "Automatic Platform Model Calibration and Tuning," which is grounded in my core research on system-level modeling. Building on this work, I have recently been awarded a subsequent SRC grant titled "Multi-dimensional Modeling, Design and Exploration of Heterogeneous Multicore SoCs" in which I collaborate with my colleague Lizy John to expand the scope, combine efforts, and create a holistic system modeling framework. Finally, since coming to UT Austin I have taken the lead on seeking collaborations to initiate new research thrusts. This has led to two collaborative NSF awards, "Formal Synthesis of Low-Energy Signal Processing Systems Relying on Controlled Timing-Error Acceptance" (with Co-PI Michael Orshansky) and "Algorithm/Architecture Co-Design of Low Power and High Performance Linear Algebra Compute Fabrics" (with Co-PI Robert van de Geijn in Computer Science).

I have also been Co-PI on smaller grants from branches of the Department of Defense (DoD), such as the Army Research Office (ARO), in which I collaborated with my colleague Robert Heath to help prototype novel wireless communication protocols in tightly constrained embedded environments. Furthermore, I generally aim to maintain a balance in my funding sources between fundamental long-term research supported by the government, more applied research supported by the DoD or national consortia tasked with creating "breakthroughs that will invent the industries of tomorrow," and direct collaborations with companies to help transfer technology and thus impact immediate industrial practice. For the latter, I continue to actively seek and cultivate (personal) connections with partners and researchers in industry. As a result, a significant portion of my work is funded through corresponding industry contracts or gifts. In many cases, competition for external funding within companies can be very selective. For example, Samsung R&D in Korea (through which I recently received funding to investigate core technologies for network and system co-simulation) only awards contracts to a handful of researchers worldwide every year.

RESEARCH RECOGNITION

My research has been internationally recognized in various forms throughout the years. While at UT Austin, my original 2003 paper on "RTOS Modeling for System-Level Design," which I wrote in my final year as Ph.D. student at UC Irvine [C8] was selected and reprinted in a 2008 book that collected the most influential contributions in the previous 10 years at the Design, Automation and Test in Europe (DATE) conference [P3]. DATE is one of the two premier conferences in my field, and arguably the premier conference most closely related to my research area. That same paper had previously been reprinted as a significant contribution in the field when it was originally published [P2].

More recently, the Ph.D. work of my student Ardavan Pedram was recognized with the Best Poster Award handed out by the IEEE Computer Society Technical Committee on Parallel Processing (TCPP) at the Ph.D. forum of the 2013 IEEE International Parallel & Distributed Processing Symposium (IPDPS). Ardavan is co-advised on my NSF grant with Robert van de Geijn in Computer Science, but since Ardavan worked with me as an ECE student before Robert joined the project and with most of this work residing in the electrical and computer engineering area, I am inherently Ardavan's main Ph.D. advisor.

Next to honors and awards, my research products have also generally received quite widespread visibility and recognition. Overall, my publications have been cited more than 2000 times with an h-index of 21 (based on Google Scholar). Our recent paper on “Predictive OS Modeling for Host-Compiled Simulation of Periodic Real-Time Task Sets” [J8] was among the top-five accessed articles of the IEEE Embedded System Letters in April, August, and November 2012. Moreover, the three books [B1, B3, B7] that I co-authored have been widely cited and are well-known in the field. I am first author on the book "System Design: A Practical Guide with SpecC" [B3], which was cited as a positive example in a panel on “Embedded Systems Education: How to Teach the Required Skills?” at the 2004 International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS). Our first two books have been translated into several other languages [B2, B4, B5], and the Japanese edition of “SpecC: Specification Language and Methodology” ranked among the top 10 bestselling technical books in Japan when it first came out. Most recently, the book " Embedded System Design: Modeling, Synthesis and Verification" (published after I joined UT Austin) is in use as a textbook for graduate classes at several universities worldwide, and its electronic version was one of the top 25% most downloaded eBooks in the relevant Springer eBook collection in 2012

INVITED PAPERS AND TALKS

Due to the interest my research has generated, I have been regularly invited to give keynotes, to submit and present papers at conferences and to give talks or present in tutorials at conferences, workshops, universities, and industry groups throughout the world. In rank at UT Austin, I have published and presented 8 invited papers at major international conferences [C43, C39, C38, C29, C27, C26, C25, C22], including three papers at the Asia and South Pacific Design Automation Conference (ASP-DAC) [C26, C25, C22], which is the premier conference in Asia for my field.

I also was invited to give a keynote at the 2011 Brazilian Symposium on Computing System Engineering (SBESC). The other two keynote talks at that event were given by Scott Brandt (a Full Professor at UC Santa Cruz) and Gernot Heiser (a Chaired Full Professor at the University of New South Wales in Australia). Throughout my career, I have presented my work in 8 conference and industry tutorials. While in rank, I was invited as a speaker in one full-day tutorial at DATE 2009. In addition to this tutorial, I have also participated in two workshops: I was invited to give a talk on my teaching experience in relation to "Developing a Class on Embedded Systems" at the Young Faculty Workshop co-located with the 2012 Design Automation Conference (DAC), and I was a presenter and panelist in a workshop on "Data Parallelism for Multi-Core Chips and GPU" organized by the IEEE Central Texas Section.

Finally, I have been invited to present at many universities and industrial research labs. Since joining UT Austin, I have given a total of 29 such invited talks worldwide. A full list of talks, workshop presentations, tutorials and keynotes can be found in my CV.

Chart of External Reviewers
Andreas Gerstlauer
Electrical and Computer Engineering Department

Name	Title	Institution	Chosen By Candidate/BC	Date Received	Reason for Declination
RECEIVED					
Arvind	Johnson Professor of Computer Science and Engineering	Massachusetts Institute of Technology	Candidate	8/10/2013	
	Conducts research in synthesis and verification of large digital systems. Conducted research in parallel computing and declarative programming languages. National Academy of Engineering. IEEE Fellow. ACM Fellow. IEEE Charles Babbage Outstanding Scientist Award. IEEE Computer Society Harry Goode Memorial Award.				
Nikil Dutt	Chancellor Professor	University of California, Irvine	Candidate	7/27/2013	
	Conducts research in embedded systems and computer-aided design, with a specific focus on the exploration, evaluation and design of domain-specific embedded systems spanning both software and hardware. IEEE Fellow. ACM Distinguished Scientist. Best Conference Paper Awards at CHDL 1989, CHDL 1991, VLSI Design 2003, CODES+ISSS 2003, CNCC 2006, ASPDAC 2006, IJCNN 2009, and DATE 2012. Past general chair for the IEEE/ACM Design				
Milos Ercegovac	Distinguished Professor	University of California, Los Angeles	BC	7/11/2013	
	Conducts research in digital arithmetic, digital design, and computer architecture. IEEE Fellow. Okawa Foundation Award 2006. Best Paper Award at ICASSAP 2004.				
Rajesh Gupta	Professor and Qualcomm Endowed Chair	University of California, San Diego	Candidate	8/7/2013	
	Conducts research in energy efficiency and mobile computing for embedded systems. IEEE Fellow. NSF Career Award. Distinguished lecturer for ACM Special Interest Group in Design Automation and IEEE Circuits and Systems Society. Editor-in-chief of IEEE Design & Test of Computers.				
Joerg Henkel	Chair for Embedded Systems	Karlsruhe Institute of Technology (Germany)	Candidate	7/28/2013	
	Conducts research on design and architectures for embedded systems with focus on low power and reliability. Best Conference Paper Awards at DATE 2008, ICCAD 2009 and CODES+ISSS 2011. Current editor-in-chief for ACM Trans. on Embedded Comp. Systems. Also chosen to give an international perspective on impact of faculty candidate's work.				
James Hoe	Professor	Carnegie Mellon University	BC	8/1/2013	
	Conducts research in computer architecture, processor microarchitecture, simulation and FPGA emulation of computer systems, and tools for high-level hardware design and synthesis. IEEE Fellow. NSF Career Award.				
Peter Hofstee	Research Staff Member	IBM	BC	7/20/2013	
	Conducts research in computer architecture. Was chief scientist and co-inventor of IBM cell broadband engine processor used in the Play Station 3. Currently researching computer system workloads for big data algorithms. Chosen to evaluate industrial impact of faculty candidate's work.				
Don Thomas	Professor	Carnegie Mellon University	BC	7/26/2013	
	Conducts research in hardware/software co-design, modeling, synthesis and computer-aided design of single-chip heterogeneous multiprocessing systems. Fellow of IEEE. Fellow of ACM. Past general chair for the IEEE/ACM Design Automation Conference.				

Chart of External Reviewers
Andreas Gerstlauer
Electrical and Computer Engineering Department

Marilyn Wolf	Rhesa "Ray" S. Farmer, Jr., Distinguished Chair in Embedded Computing Systems	Georgia Institute of Technology	Candidate	7/26/2013	
	Conducts research in embedded computing, ranging from hardware/software co-design algorithms and real-time scheduling algorithms to code compression and distributed smart cameras. Fellow of IEEE. Fellow of ACM. IEEE Computer Society Golden Core Award. ASEE Frederick E. Terman Teaching Award. IEEE Circuits and Systems Society Education Award.				
Martin Wong	Professor	University of Illinois, Champaign-Urbana	BC	8/19/2013	
	Conducts research in combinatorial optimization, design and analysis of algorithms, field-programmable systems, design for manufacturing, CAD for VLSI electronic packaging and computer-aided design of VLSI circuits. IEEE Fellow. Best Conference Paper Awards at DAC 1986 and ICCD 1995. CAD Transactions Best Paper Award 2000. Best-of-20-Years ICCAD Paper 2002. Distinguished Lecturer for IEEE Circuits and Systems Society.				
Decline	none				
No response	none				

COCKRELL SCHOOL OF ENGINEERING
THE UNIVERSITY OF TEXAS AT AUSTIN

Department of Electrical and Computer Engineering • Engineering Science Building
1 University Station C0803 • Austin, Texas 78712-0240 • (512) 471-6179 • Fax (512) 471-3652

June 19, 2013

Dear Dr. Wong:

The Department of Electrical and Computer Engineering is considering Dr. Andreas Gerstlauer for tenure and advancement in rank to the position of Associate Professor at The University of Texas at Austin. The two main criteria for promotion are demonstrated scholarship and excellent teaching. We would particularly appreciate your candid assessment of his scholarly contributions. Although we recognize it is unlikely that you have firsthand knowledge of his teaching, any information you do have with this respect to this would also be welcome. A copy of the candidate's curriculum vitae is enclosed. To provide context, I should note that The University of Texas at Austin normally considers a faculty member for promotion to Associate Professor upon completion of five years in probationary status. Professor Gerstlauer has accumulated five years of service in probationary status, so this review is taking place at the normal time for tenure evaluation.

Your assessment of Professor Gerstlauer would be most helpful if you could address the following questions:

1. Do you know Professor Gerstlauer, and if so, for how long and under what circumstances?
2. How would you assess the contributions to your discipline made by Professor Gerstlauer's publications? Which publications would you judge to be the most significant, and why?
3. How would you assess Professor Gerstlauer's development as a scholar/researcher compared with others in his cohort at research-intensive universities?
4. What is your perspective on Professor Gerstlauer's promise for further growth and significant contributions to his field?

The following link provides you access to Professor Gerstlauer's CV, recent publications and research and teaching statements to assist you in this task:

To access the site please use the following login and password:

Website: https://fuze1.ece.utexas.edu/eceapps/promotion
Login: cand0406
Password: uWEDem

Please let us know if you prefer to receive this material via email or regular mail.

We would be grateful for any additional comments you might have.

Under the laws of the State of Texas, Professor Gerstlauer has the right to request to see any materials in his personnel file, including your letter. Although Professor Gerstlauer has waived that right, it is not clear whether he can reinstate that right at some future time. It is also the case that the members of our internal review committees will see your letter as part of the promotion process. They will hold the comments you make in confidence. Please know that we will make every attempt to hold the contents of your letter confidential within all limits of the law.

We would appreciate receiving your letter no later than July 20, 2013. Please enclose a copy of a short version of your curriculum vitae or résumé (preferably no longer than one page) or the URL for your Website where we may obtain this information. While electronic letters or PDF are fine, our guidelines require that you either sign your letter or include an electronic signature. If you have any questions about this, please do not hesitate to contact me at your convenience at 512-471-6971.

I want to personally thank you for your time and assistance with this important matter. I recognize that the amount of time required to do a thoughtful review is considerable.

Sincerely,

Dr. Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering
The University of Texas at Austin
Austin, Texas 78712-0240

FIVE SIGNIFICANT WORKS

All references to publications are indexed on the resume, where [Jxx] is used to indicate journal articles, [Cxx] conference papers, [Pxx] book chapters, and [Bxx] books.

List of five most significant publications while in rank

J5. A. Gerstlauer, C. Haubelt, A. D. Pimentel, T. P. Stefanov, D. D. Gajski, J. Teich, "Electronic System-Level Synthesis Methodologies," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 28, no. 10, pp. 1517-1530, October 2009.

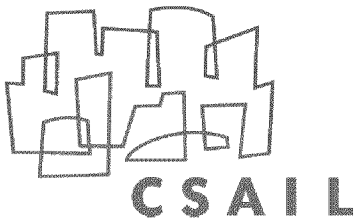
J6. G. Schirner, A. Gerstlauer, R. Dömer, "Fast and Accurate Processor Models for Efficient MPSoC Design," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 15, no. 2, article no. 10, pp. 1-26, February 2010.

J8. P. Razaghi, A. Gerstlauer, "Predictive OS Modeling for Host-Compiled Simulation of Periodic Real-Time Task Sets," *IEEE Embedded System Letters*, vol. 4, no. 1, pp. 5-8, March 2012.

J9. A. Pedram, R. A. van de Geijn, A. Gerstlauer, "Codesign Tradeoffs for High-Performance, Low-Power Linear Algebra Architectures," *IEEE Transactions on Computers (TC)*, special issue on Energy Efficient Computing, vol. 61, no. 12, pp. 1724-1736, December 2012.

J11. K. He, A. Gerstlauer, M. Orshansky, "Circuit-Level Timing-Error Acceptance for Design of Energy-Efficient DCT/IDCT-based Systems," *IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)*, vol. 23, no. 6, pp. 961-974, June 2013.

MIT COMPUTER SCIENCE AND ARTIFICIAL INTELLIGENCE LABORATORY



August 10, 2013

Dr. Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering
The University of Texas at Austin
Austin, Texas 78712-0240

Reference: Promotion of Dr Andreas Gerstlauer

Dear Ahmed,

I recommend that Dr Andreas Gerstlauer be promoted to the rank of Associate Professor with tenure. I met Andreas when he was a graduate student working under Professor Dan Gajski, whom I have known for a very very long time. At some stage, though I do not know exactly when, I became aware that Andreas was an important member of the SpecC project, which was Gajski's flagship project. I have seen Andreas periodically at various meetings and at UT Austin because of our common interest in Electronic System-Level design of embedded computer systems (ESL). I regard ESL as an extremely important area of research because the fruits of Morse law are not realizable without commensurate progress in our ability to design systems whose complexity increases every year.

Though Andreas has worked on several aspects of the ESL problem, his primary focus has been on tools for modeling systems-on-a-chip (e.g., smart phones, tablets, ...). The complexity of such chips is mind boggling – they not only contain small multicore processors but also have 80 to 100 specialized hardware blocks to reduce power consumption and provide desirable performance. Sometimes the complexity of these specialized blocks matches the complexity of multicore processors on the same chip. A persistent concern in the design of such complex systems is if it would work when fabricated. Will it be able to support important *use scenarios*? Will busses get clogged, or OS scheduling fail to respond in time for a proper user experience. The primary technique to ascertain the answers to such questions is to simulate the system with software running on an accurate model of the hardware.

This is easier said than done. Over the last decade models of many components of such systems have become available in SystemC or its precursor SpecC. Nevertheless the speed of accurate simulations is so slow that one never gets to execute the scenarios of interest on the simulation models. Consequently, researchers have devised techniques to make simulations run extremely fast at the expense of modeling accuracy. Within the field, there is endless debate about the accuracy of simulations – Can we trust the results? – Has one taken all the important factors into account? Of course the debate goes on because no one knows the right answer until the chip is actually built and tested!

The Stata Center, Building 32 – G866 , **32 Vassar Street, Cambridge, Massachusetts** 02139 **Phone** +1.617.253.6090 **Fax** +1.617.253.6652

Andreas primary research contributions are in the area of very fast modeling where the OS effects (e.g., scheduling, interrupts) and the processor's micro-architectural features are taken into account. Since I was not familiar with the details of Andreas' work, I took this opportunity to read the five papers he had selected to represent his most important contributions. Here are my brief comments on these papers:

1. Electronic System-Level Synthesis Methodologies (2009): This paper is an in-depth classification of ESL design tools, and points out that a complete ESL design flow requires both RTL synthesis and HW/SW codesign. C-based solutions (SystemC, SpecC) have a lot of appeal because systems people already know C, one can express time-independent behavior in C, C-based simulation environments are simpler and cheaper, and implementations and models of many components and algorithms are often available in C. However, time-independence is also an albatross and has made good hardware synthesis from C-based solutions elusive. This paper does not contain new results but offers an important taxonomy of tools; it is likely to be cited widely.

2. Fast and Accurate Processor Models for Effcient MPSoC Design (2010): I approached this paper with great anticipation because the topic is very close to my own research. (I have been advocating and building fast cycle-accurate models of processors to run on FPGAs). It turned out that this paper offers a completely different approach which made me think of the limitations of my own approach for Systems-on-a-chip simulations. Just to avoid confusion, it is important to state that Andreas' and my notion of accurate models are very different. I have been extremely critical of published simulation results in the architecture conferences on the ground that modeling errors are so large that claims like "solution x is better than solution y by (say) 5%" are bogus. Andreas on the other hand is starting at the other extreme of un-timed models and showing how time (or modeling realism) can be introduced layer by layer to dramatically increase the usefulness of SystemC models. There is a fairly creative factoring of problems in simulation of time in Andreas approach – a detailed description of which is beyond the scope of this letter. I would recommend this paper to my students and others who are interested in simulation and modeling.

3. Predictive OS Modeling for Host-Compiled Simulation of Periodic Real-Time Task Sets (2011): In some sense this paper is related to the paper on Processor modeling. He is proposing *Host-Compiled simulations* which to me is the same thing as *direct execution models* and which are used extensively in the architecture community. Host-Compiled simulations may not be a novel idea but how Andreas used it to model OS/Architercture/application interaction is certainly creative. He showed how the application code can be back annotated for interrupts and systems calls and how during execution, an accurate timing model can be injected at these points to make the whole simulation much more realistic. I think this idea is likely to be copied by many simulators.

4. Circuit-Level Timing-Error Acceptance for Design of Energy-Efficient DCT/IDCT-Based Systems (2013): Circuits consume less power if operated at a lower voltage but also generate more errors. The central idea in this paper is that for some applications answers degrade gradually as we accept more and more errors, and therefore we can trade accuracy for less power. Video processing seems like an ideal application to try out this idea – who cares about a few errors in a video frame? This paper reports on a well-executed study of an important component in video processing and shows that the power consumption can be reduced by as much as 70% by accepting a very small amount of error. A new idea in the paper was to do some post processing corrections

to reduce the amount of errors. This is an important enough application that people are likely to read and cite this paper.

5. Codesign Tradeoffs for High-Performance, Low-Power Linear Algebra Architectures (2012): This paper is a study of how much Linear Algebra processing can benefit from special-purpose hardware support. The short answer is a lot provided one focusses on minimizing data movement in the memory hierarchy. The study is well executed and has involved some design effort. The results were consistent with my expectations.

I found all five papers to be well written and full of proper references to related work. There is a good balance between *tools* versus *design* papers. For me Andreas work would lack credibility without the design papers. The topics covered by these papers are of central concern in ESL. I also found the architecture modeling paper and the OS paper together offering some creative insights in a difficult modeling question. I rarely participate in the program committees (PCs) of ESL/CAD conferences, and therefore, it is difficult for me gauge what the broader community thinks of Andreas work. However, based on his long list of publications and his regular participation in the PCs of important CAD conferences, he must have a solid reputation in the field. He also seems to be successful in raising research funds.

Based on all this information I am happy to recommend that Andreas be granted tenure and promoted to the rank of Associate Professor.

Sincerely,

Arvind
Johnson Professor of Computer Science and Engineering

Biography: Arvind is the Johnson Professor of Computer Science and Engineering at MIT. Arvind's group, in collaboration with Motorola, built the Monsoon dataflow machines and its associated software in the late eighties. In 2000, Arvind started Sandburst which was sold to Broadcom in 2006. In 2003, Arvind co-founded Bluespec Inc., an EDA company to produce a set of tools for high-level synthesis. In 2001, Dr. R. S. Nikhil and Arvind published the book "Implicit parallel programming in pH". Arvind's current research focus is on enabling rapid development of embedded systems. Arvind is a Fellow of IEEE and ACM, and a member of the National Academy of Engineering and the American Academy of Arts and Sciences.

Jilda Gayle

From: Arvind <arvind@csail.mit.edu>
Sent: Monday, August 12, 2013 2:17 AM
To: Bearden, Carole A
Cc: Tewfik, Ahmed H; Jilda Bolton (jildagayle@gmail.com); Sally O Lee
Subject: Re: Letter of reference for Dr. Andreas Gerstlauer
Attachments: 130710AndreasGerstlauer.pdf

Hi Carole

The letter for Andreas is attached. Please let Sally know if you also need a hard copy.

Thanks
Arvind

On Wed, Jun 19, 2013 at 12:16 PM, Bearden, Carole A <cjb@mail.utexas.edu> wrote:

Dr. Arvind,

Thank you for your support of Dr. Andreas Gerstlauer promotion and agreeing to write a recommendation letter. Attached is a formal request for the letter with a website, logon and password to access his information as well as his CV.

Best regards,

Carole Bearden

Executive Assistant

The University of Texas at Austin

Electrical and Computer Engineering

ENS Room 236
2501 Speedway, C0803

Austin, Texas 78712-0240 USA

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July 27, 2013

Dr. Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering
The University of Texas at Austin
Austin, Texas 78712-0240
Email: tewfik@austin.utexas.edu

Dear Professor Tewfik,

RE: Letter of evaluation for tenure promotion of Dr. Andreas Gerstlauer to Associate Professor.

I'm delighted to write a letter of evaluation for the appointment of Dr. Andreas Gerstlauer to Associate Professor. At the very outset, let me state my strong support for the tenure promotion of Dr. Gerstlauer. Per your request, my letter will address the specific questions asked.

a. How long I've known Dr. Gerstlauer

I have known Dr. Gerstlauer since he entered the PhD program in computer science at UCI in 1997 (I actually spotted his application when I served on the graduate admission committee and championed his case for admission). Note however that he did not affiliate with my research group (he joined Dan Gajski's group) and I did not serve on his dissertation thesis committee, nor did I have any research publications with him. He did however take a couple of graduate courses with me (where he performed very well), and I have subsequently followed some of his work through his dissertation, post-doctoral, and tenure-track phases of his career. I have been impressed by the consistent intellectual quality of his work, his taste in selecting important problems, and his ability to create research artifacts that have lasting impact. I address these items in the rest of my letter.

b. Contributions to the field and quality of publications

Dr. Gerstlauer's research is in embedded systems, with a focus on early system-level specification, and the tools and methodologies to convert these high-level specifications into working hardware/software implementations while satisfying stringent multi-dimensional

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constraints (e.g., performance, power, energy, reliability, etc.). While many embedded systems are application- or domain-specific, we are increasingly seeing the use of embedded system design methodologies being deployed in the main stream high performance computing arena, as the power/energy/reliability and other careabouts begin to converge across these design flows. This requires new abstractions, models, optimizations and compilation flows for the reliable and efficient deployment of such low-power embedded and high-performance systems.

Towards this end, Dr. Gerstlauer has already made an impressively strong impact through the development and distribution of models and tools for early System Level Design (SLD), and for the exploration and mapping of these models onto heterogeneous multiprocessor platforms. To wit, I believe Dr. Gerstlauer is the key intellectual contributor behind the SpecC modeling language and methodology, which (besides the high citation counts) led to development of semantics for the SystemC language, which is now the default industry standard specification language for mixed hardware/software design implementations. The impact of this work is impressive, particularly coming from a researcher who is so early in his career. After joining UT Austin, Dr. Gerstlauer has continued to build on this momentum by creating abstractions for RTOS modeling for heterogeneous multi-core platforms, hardware-dependent software design methodologies, and transaction-level modeling for efficient exploration of communication architectures. His recent work on speeding up system-level simulation and embedded software modeling already show early signs of impact both in the research arena, as well as for industrial practitioners.

The overall quality of Dr. Gerstlauer's research is extremely strong, as evidenced by the high-quality venues where his work has appeared. His archival journal articles appear in the most prestigious ACM and IEEE journals, including ACM Transactions on Design Automation of Electronic Systems (ACM TODAES), IEEE Transactions on Computers, IEEE Transactions on Computer-Aided Design of Circuits and Systems (IEEE TCAD), IEEE Transactions on VLSI Systems (IEEE TVLSI), and IEEE Embedded Systems Letters, to name a few. There are no better journals for publication in these research areas.

Moreover, it is important to note that in the embedded systems arena, premier refereed conferences are the preferred outlet for research publications. Dr. Gerstlauer's publications have appeared in highly selective peer-reviewed conferences that typically have acceptance rates of 12-30% with each paper being reviewed by anywhere between 3-6 reviewers. **Publication in such premier conferences and workshops is often considered to be on par with the best archival journals, and is one of the primary means of research dissemination.** Towards this end, Dr. Gerstlauer has a very strong record of publication in premier conferences and workshops; indeed his papers have appeared in the leading peer-reviewed conference venues including: DAC,

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DATE, CODES+ISSS, ICCAD, ASPDAC, and ASAP, to name a few. Again, there are no better premier conferences for publication in his area of research.

As I mentioned earlier, Dr. Gerstlauer's research is in the general area of embedded systems: this is an exciting and vibrant area of research with the potential for both short term industrial impact (which he has already demonstrated through his SpecC and SER projects), as well as long-term societal impact through the development of technologies that will aid humanity in terms of integrating embedded computing into our daily social fabric of our lives. The challenges resulting from the design of embedded computing systems differ quite radically from traditional computing systems, in that one not only has to deal with problems of performance, power and energy, but also requires explicit representation and interaction with the physical environment in which these embedded systems are deployed. The resulting problems often require balancing multi-dimensional constraints that often interact with each other in complex and non-intuitive ways. The resulting problems are extremely challenging and require intellectual depth together with strong engineering design. Thus there is no question that Dr. Gerstlauer is tackling problems on the cutting edge of research, and providing solutions to substantive questions that advance the state of the art in embedded systems.

c. Development as a scholar/researcher and peer group comparison

Dr. Gertslauer's choice in pursuing challenging and important problems, and a successful track record of creating tools and methodologies that not only have impact in research, but in commercial deployment all show a level of capability and maturity that places him at the level of a scholar who is well beyond tenure. Indeed I would place ahead of recently tenured Associate Professors such as Azadeh Davoodi at Wisconsin, Deming Chen at Illinois, and Roman Lysecky at University of Arizona; and place him the cohort of emerging star Associate Professors such as David Atienza at EPFL and Vijay Raghunathan at Purdue.

d. Future growth and potential

Professionally, Dr. Gerstlauer is already operating at the level of an Associate Professor: he served as Topic or Track Chair for DAC and CODES+ISSS; and has co-organized or Co-Chaired events such as VLSI-SoC and Embedded MultiProcessor Software Synthesis Workshop at DAC. And of course he serves on, or has served on the Technical Program Committees of key international conferences in embedded systems and EDA (e.g., DATE, DAC, ICCAD, CASES, CODES+ISSS and RTAS). I expect that he will continue to be asked to serve on other Technical Program Committees, and also will be asked to lead major events in the future. Thus Dr. Gerstlauer is performing valuable professional service to the profession. In terms of research, I

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Chancellor's Professor
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Email: dutt@uci.edu

believe that Dr. Gerstlauer's recent forays into hardware-software codesign for high-performance linear algebra computations, and mixed simulation frameworks for CyberPhysical Systems all point to his growing momentum for selecting important intellectual challenges and creating innovative solutions with the potential for high research as well as practical impact. There's no doubt in my mind that Dr. Gerstlauer's profile is already at the level of a successful tenured researcher in the embedded systems arena. Indeed, with his record Dr. Gerstlauer would have no problem gaining tenure in my school and within the University of California system.

Summary

I believe Dr. Gerstlauer is on the trajectory towards an exciting and productive intellectual career in academia, and I believe he will continue to push into new research frontiers, using a combination of modeling, analytical and algorithmic techniques to aid future embedded system designers. **I'm delighted to give my enthusiastic and unqualified support for the tenure promotion of Dr. Andreas Gerstlauer to Associate Professor.**

Please do not hesitate to contact me if you have further questions.

Sincerely,

Nikil Dutt
Chancellor's Professor
Department of Computer Science (primary)
Department of EECS
Department of Cognitive Sciences

Jilda Gayle

From: nikildutt@gmail.com on behalf of Nikil Dutt <dutt@ics.uci.edu>
Sent: Saturday, July 27, 2013 2:13 AM
To: Bearden, Carole A; Tewfik, Ahmed H; Jilda Bolton (jildagayle@gmail.com)
Subject: Re: Letter of reference for Dr. Andreas Gerstlauer
Attachments: andreas-gerstlauer-tenure.pdf

Dear Prof. Tewfik,

Please find attached a letter of reference for the tenure promotion of Dr. Andreas Gertlauer.

All the best,

Nik Dutt

On Wed, Jun 19, 2013 at 9:34 AM, Bearden, Carole A <cjjp@mail.utexas.edu> wrote:

Dr. Dutt,

Thank you for your support of Dr. Andreas Gerstlauer promotion and agreeing to write a recommendation letter. Attached is a formal request for the letter with a website, logon and password to access his information as well as his CV.

Best regards,

Carole Bearden

Executive Assistant

The University of Texas at Austin

Electrical and Computer Engineering

ENS Room 236
2501 Speedway, C0803

Austin, Texas 78712-0240 USA

UNIVERSITY OF CALIFORNIA, IRVINE

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Nikil D. Dutt
Chancellor's Professor
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Short Biography of Nikil Dutt

Nikil D. Dutt is a Chancellor's Professor at the University of California, Irvine, with academic appointments in the CS, EECS and Cognitive Sciences departments. He received a B.E.(Hons) in Mechanical Engineering from the Birla Institute of Technology and Science, Pilani, India in 1980, an M.S. in Computer Science from the Pennsylvania State University in 1983, and a Ph.D. in Computer Science from the University of Illinois at Urbana-Champaign in 1989. He is affiliated with the following Centers at UCI: Center for Embedded Computer Systems (CECS), California Institute for Telecommunications and Information Technology (Calit2), and the Center for Pervasive Communications and Computing (CPCC).

Professor Dutt's research interests are in embedded systems, electronic design automation, computer architecture, optimizing compilers, system specification techniques, distributed systems, and brain-inspired computing. He is a coauthor of seven books and over 300 journal and refereed conference articles. His research has also been recognized by Best Paper Awards at the following conferences: *CHDL'89, CHDL'91, VLSI Design 2003, CODES+ISSS 2003, CNCC 2006, ASPDAC 2006, IJCNN 2009, and DATE 2012*; and Best Paper Award Nominations at: *WASP 2004, DAC 2005, VLSI Design 2006*, and *CODES+ISSS 2011*. He has also received a number of departmental and campus awards for excellence in teaching at UC Irvine.

Professor Dutt served as Editor-in-Chief of ACM Transactions on Design Automation of Electronic Systems (TODAES) between 2003-2008 and currently serves as Associate Editor of ACM Transactions on Embedded Computer Systems (TECS) and of IEEE Transactions on VLSI Systems (TVLSI). He was an ACM SIGDA Distinguished Lecturer during 2001-2002, and an IEEE Computer Society Distinguished Visitor for 2003-2005. He has served on the steering, organizing, and program committees of several premier CAD and Embedded System conferences and workshops, including ASPDAC, DAC, DATE, ICCAD, CODES+ISSS, CASES, ISLPED and LCTES. He is a Fellow of the IEEE, an ACM Distinguished Scientist, and an IFIP Golden Core awardee.

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July 11, 2013

Dr. Ahmed Tewfik
Chairman, Department of Electrical and Computer Engineering
The University of Texas at Austin
Austin, Texas 78712-0240

Dear Professor Tewfik,

This is my letter of recommendation for Prof. Andreas Gerstlauer for his promotion to Associate Professor with tenure. I have known about his research in system-level design and application-specific architectures for several years. We met only recently: at the 22nd IEEE Conference on Application-Specific Systems, Architectures and Processors, in Santa Monica, California, September 11-14, 2011, and at the IEEE Symposium on Computer Arithmetic, Austin, Texas, April 2013. Most recently I invited Prof. Gerstlauer to give a seminar on his research in Computer Science Department at UCLA. These interactions have given me an opportunity to observe his technical work, discuss research ideas, listen to his presentations, and follow his professional activities. He is excellent in all these categories. I have a strong appreciation of his technical contributions: he selects to work on good problems, his ideas have originality, and he carries out his work from a formal level through implementation details. His research is of a definite practical importance. His skills, dedication and energy are also strong. He is a very engaging speaker – I believe that he must be an excellent teacher and mentor. He is also a good communicator, easy to get along with, and highly personable.

Prof. Gerstlauer's research has contributed to several areas in computer architecture and design automation. He is currently focusing on an important and timely area: automating exploration and synthesis of high-level specifications on modern multiprocessor architectures. He is working on problems arising in integrating general-purpose and embedded systems, both at the software and hardware levels. This architectural heterogeneity seems to be essential in addressing rising costs of design, power reduction, and reliability. He and his students have made notable contributions in solving programmability problems in reconfigurable computing. He has also made excellent contributions in the design of energy-efficient systems by reducing the overheads in computations. His approach exploits the use of domain specialization and heterogeneity. A good example of such a work in his research group is an algorithm/hardware co-design of a linear algebra processor, published in the IEEE Transactions on Computers, 2012, which achieves several orders of magnitude better efficiency than current architectures. The results were published in the IEEE Transactions on Computers (Special Issue on Energy Efficient Computing). This work has also attracted attention from IBM and AMD as well as Stanford and University of Wisconsin, resulting in research collaboration. Approximate arithmetic is a rising approach in reducing energy consumption: Prof. Gerstlauer showed with his coworkers in a recent ICCAD paper (2012) how to model and synthesize energy-optimal adders with good performance. He and his

collaborators have recently proposed a novel strategy to exploit timing error acceptance (TERRA) in image and video processing systems to significantly increase energy efficiency, published in the IEEE Transactions on Circuits and Systems for Video Technology, 2013. These works are typical of his research: there is a clear, original idea, a good technical depth, and strong experimental results. Prof. Gerstlauer and his collaborators made notable contributions in identifying key principles of electronic system design, covering both hardware and software aspects. This important paper was published in the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, and had an influence on subsequent research in this area.

Prof. Gerstlauer has a very strong publication record in key journals and conferences. His work has been published in IEEE and ACM publications, such as the IEEE Transactions on Computers, IEEE Transactions on VLSI, IEEE Transactions on CAD, and ACM Transactions on Design Automation of Electronic Systems. He and his collaborators have also extensively published in leading (reviewed) conferences such as the ICCAD, IEEE Symposium on Arithmetic, DATE, and IEEE ASAP. Their 2003 paper on RTOS modeling for system level design has been included in The Most Influential Papers of 10 Year od DATE. All of these venues are highly competitive and frequent presence of Prof. Gerstlauer's in these publications attests to the quality of his research. His record in obtaining funding appears adequate to support his research group.

Prof. Gerstlauer's vision of research plans is well articulated and I agree with his characterization of outstanding problems related to managing design complexity, dealing with progress in energy-efficient systems, technology, and design automation at the high level. All of these problems provide challenging opportunities for cutting-edge research. Based on his past accomplishments, I believe that Prof. Gerstlauer will continue being successful in achieving these goals.

Prof. Gerstlauer's participation at various international and domestic conferences has been strong and recognized. He has participated in a large number of technical program committees that attests to his wide recognition by peers – domestic as well as international. He has also given keynote presentations at international conferences, clearly indicating that he is well recognized in the world research community. He has very strong professional involvement in a large number of technical program committees, in awards committees, and as reviewer for the National Science Foundation, DOE, and several leading IEEE and ACM journals and transactions. From his self-serving letter I also see that he has a strong record in teaching and advising PhD and MS students. Judging by very nicely delivered conference presentations I heard, he must be a very good instructor. His service to the university seems strong.

In summary, based on his excellent scholarly achievements, professional recognition, strong student mentoring, and strong professional activities and University service, I strongly recommend promoting Prof. Gerstlauer to Associate Professor with tenure. His overall record would qualify him for such a promotion at UCLA. I would certainly be happy to have such a productive and capable colleague in my department.

Sincerely

Milos D. Ercegovac
Distinguished Professor of Computer Science

Jilda Gayle

From: Tewfik, Ahmed H <tewfik@austin.utexas.edu>
Sent: Friday, July 19, 2013 5:18 PM
To: Milos Ercegovac; Bearden, Carole A
Cc: Jilda Bolton (jildagayle@gmail.com)
Subject: RE: Letter of reference for Dr. Andreas Gerstlauer

Many thanks Milos!

We greatly appreciate your support.

Regards,
Ahmed

From: Milos Ercegovac [mailto:milos@cs.ucla.edu]
Sent: Friday, July 19, 2013 5:04 PM
To: Bearden, Carole A
Cc: Tewfik, Ahmed H; Jilda Bolton (jildagayle@gmail.com)
Subject: Re: Letter of reference for Dr. Andreas Gerstlauer
Importance: High

Dear Dr. Tewfik,

Attached is my recommendation letter for the promotion of Prof. Andreas Gerstlauer.
I hope it helps.

Sincerely,

Milos Ercegovac

Short Biography

Prof. Miloš D. Ercegovac
Computer Science Department
University of California at Los Angeles
E-mail: milos@cs.ucla.edu
http://www.cs.ucla.edu/~milos/

Dr. Miloš D. Ercegovac is a Distinguished Professor and a former Chair in the Computer Science Department of the Henry Samueli School of Engineering and Applied Science, University of California at Los Angeles, where he has been on the faculty since 1975. He earned his MS ('72) and PhD ('75) in computer science from the University of Illinois, Urbana-Champaign, and BS in electrical engineering ('65) from the University of Belgrade, Serbia. Dr. Ercegovac has specialized for over 40 years in research and teaching in digital arithmetic, digital and computer system design, and parallel architectures, extensively published in the leading journals and conferences. His dedication to teaching and research has also resulted in several co-authored books: two in the area of digital design (*Digital Systems and Hardware/Firmware Algorithms*, Wiley & Sons, 1985, and *Introduction to Digital Design*, Wiley & Sons, 1999), and two in digital arithmetic (*Division and Square Root: Digit-Recurrence Algorithms and Implementations*, Kluwer Academic Publishers, 1994, and *Digital Arithmetic*, Morgan Kaufmann Publishers - a Division of Elsevier, 2004.) He received the Lockheed-Martin Excellence in Teaching award in 2009. He is also recipient of the 2013 Distinguished Alumni Educator Award from the Department of Computer Science at the University of Illinois at Urbana-Champaign. Dr. Ercegovac has been involved in organizing the IEEE Symposia on Computer Arithmetic since 1978. He served as an associate editor of the IEEE Transactions on Computers 1988 -1992 and as a subject area editor for the Journal of Parallel and Distributed Computing 1986 -1993. Dr. Ercegovac's work has been recognized by his election in 2003 to IEEE Fellow and to Foreign Member of the Serbian Academy of Sciences and Arts in Belgrade, Serbia. He is also a member of the ACM and of the IEEE Computer Society.

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August 7, 2013

Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering
The University of Texas at Austin
Austin, Texas 78712-0240

Subject: Andreas Gerstlauer

I am writing this letter in response to your request of June 28, 2013 regarding evaluation of Professor Andreas Gerstlauer for promotion and tenure to Associate Professor. I have known Dr. Gerstlauer since 1998, first as a student in my class at Irvine and later as a graduate student in the department. I have not collaborated or co-authored on any projects, paper or proposal with him. For the sake of concision first I will make general remarks about the nature of Professor Gerstlauer's research followed by answers to specific questions in your letter.

Professor Andreas Gerstlauer's research is in the sub-area of system-level design in Embedded Systems. Research in this area borrows from the intellectual tradition in electronic design automation (or VLSI/CAD) with publishing forums that consist of an eclectic mixture of traditional CAD forums as well as a number of new (and unproven) forums in Embedded Systems. There is generally no singular driving problem – at least in the sense of engineering design and optimization – that a typical researcher seeks to address in all of his/her work. Instead, there are guiding goals that serve as an organizing umbrella for individual researchers. These may include "improving level abstraction in design, synthesis or verification" or "reducing power or energy." Progress is made through contributions in specific models and methods that sometimes show up as tools and/or languages for the practitioner. While most efforts result in a publication or two in various forums that are somewhat rank ordered, a few projects that make it to the practitioners as tools are considered the most impactful. Sometimes, tools or other artifacts are produced by a broader community or a different unrelated group, thus obscuring 'research credit' especially for a junior researcher.

When it comes to forums and metrics, the publication culture in this domain is truly at the intersection of entirely-conference-centric computer science research and primarily-conference-centric computer engineering (part of electrical engineering) research. In other words, conferences are primary means for disseminating results: the paper lengths in Tier 1 forums tend to be 6-14 pages (another interpolation of two cultures) that are selected through highly competitive review processes that admit no second chances or revisions. While VLSI/CAD publications have more journal forums, embedded systems is somewhere in between for its balance with conferences and journals. Further, embedded systems forums, like the area, are still a work-in-progress: some of the prominent work shows up in forums that reflect the intellectual training and background of the researchers: that would be VLSI/CAD for Andreas. Other researchers in embedded systems

may well publish similar work (in terms of topic) in computer architecture, signal processing or real-time systems conferences. Thus, the choice of the 'host' forum should be treated without prejudice since it reflects primarily a community affinity more than true rank ordering of the quality of contribution. It also means that typical embedded systems researchers tend to 'flip around' forums among these domains which ultimately reflects evolving nature and collaboration of their research, but it also hurts their citation counts by changing the peer communities and thus visibility of their work. Citation counts and h-indices are useful measures here only to the extent you use them to compare researchers in embedded systems area.

For someone with Professor Gerstlauer's intellectual persuasion, the prominent 'host' forums are: DAC, DATE, ICCAD and ASP-DAC. They are listed in no particular order, especially for the "system design EDA" researchers who tend to be somewhat less prominent part of these forums. Among these, DATE is perhaps most progressive of the system design research, followed by ASP-DAC. ICCAD most definitely does a token 'metoo' job in system level design, while presenting a strong research results in more mainstream EDA topics related to physical, logical level design and verification. Among journals, embedded systems research shows up in IEEE Transactions on CAD/CAS, IEEE Transactions on VLSI, ACM TODAES, IEEE Transactions on Computers and ACM TECS. Paucity of decent forums led the community to start IEEE Embedded Systems Letters. As founding EIC of IEEE ESL, I know a bit more about it than others: the acceptance rate has varied from 14% in the first year to about low 20s now. Thus the primary places where we expect to see research results by Professor Gerstlauer would be one of the ESWeek forums (such as CODES+ISSS or EMSoft or CASES), DATE, DAC and ASP-DAC. For the topical area that Prof. Gerstlauer works on these are roughly in the class. Given his background, Professor Gerstlauer's work also shows up (often) in an IFIP forum on Embedded Systems (IESS). I don't know much about the quality of this forum, I have not attended it, but I suspect it is somewhere between Tier 1 and Tier 2.

I will note that there was a period of about 3-4 years between his graduation from Irvine to joining UT when he worked as a postdoc to Daniel Gajski on a Japanese project. Given the nature of the contract and work, I suspect the emphasis was strongly on implementation that must have come at the cost of his publication record. However, I do know it was a period of his intellectual growth and perhaps the work that he would be known best for around that time: SpecC since he produced that artifact that I talked about earlier. Along with Reiner Doemer he had made SpecC happen, though I suspect that Andreas probably has claim to a large share of the credit.

Let me now address the questions posed in your letter:

- *How would you assess the contributions to your discipline made by Professor Gerstlauer's publications? Which publications would you judge to be the most significant, and why?*

This question understates the mechanisms by which an academic makes an impact by implying publications to be the sole expression. Professor Gerstlauer's publication record is strong both in the aggregate as measured by the numbers, in quality as measured by best paper nominations/awards and in impact as measured by transition to practice. Among the papers that stand out are OS Modeling paper that appeared in DATE 2003 and more recently his IEEE ESL paper in 2012. The notion of host-compiled models is certainly interesting and came at the right time just when the community was looking into building and using transactional models for system-level design. These have already made into the practice and as standards in things like SystemC.

While Andreas has a number of contributions in system level modeling and simulation area – not surprising given his background and training – I am most intrigued and heartened by his work with Michael Orshansky on approximate computing (their paper in IEEE TCSVT 2012). He has pursued both circuit level and numerical/signal processing strategies to enable approximate computing. He has pursued this line with the goal to reduce power consumption. I find this work no-

table for two reasons: one, it demonstrates, Professor Gerstlauer's willingness and ability to pursue topics far outside his training and comfort zone as a 'system-level CAD' researcher; two, he has chosen a set of problems in an area of tremendous current importance that is showing up in a wide range of strategies from devices and circuits (where it goes by 'variability-aware design'), programming languages ('principled approximation') to data bases (such as BlinkDB).

- *How would you assess Professor Gerstlauer's development as a scholar/researcher compared with others in his cohort at research-intensive universities?*

Professor Gerstlauer's has made notable attempts at expanding his research portfolio from purely system-level EDA problems. This is both practical and strategic. For one, there is limited funding support for EDA and even (much) less for system-level modeling and EDA. Strategically, it is important for Professor Gerstlauer to build a research portfolio that will 'move the needle' in system-level design practice through innovations that involve technologists beyond EDA algorithms and tools. There is evidence that Professor Gerstlauer has built a research portfolio that goes from signal processing, numerical methods to circuits giving him opportunities to approach a diversity of funding sources in support of his research.

Peer comparisons are hard and sometimes in appropriate because there is really no singular cohort. Even among researchers within his academic age, there is diversity of experience, time taken to do something else et cetra. For instance, a gap of nearly four years in Professor Gerstlauer's academic CV may show up as fewer publications than his post-PhD cohort will indicate but makes him a stronger researcher for the artifact that he produced during this period. I am sure others have similar characteristics making peer comparison especially difficult. While I try to avoid putting down any names to compare some kind of rank ordering of researchers in his age group, I will say this: with an h-index of 21 and a citation count of over 2000, Professor Gerstlauer is among top half a dozen researchers in system-level CAD area. In terms of publication counts, he is likely to be overshadowed by researchers in physical or logical design CAD area simply because of the publishing culture. (There is nearly an inverse relationship of publication counts and the level of abstraction in the electronic design automation area). On the other hand, there is a limited number of researchers in system-level CAD area and among these Professor Gerstlauer is likely among the top three. These include researchers such as Hiren Patel at Waterloo (somewhat junior), Steve Edwards at Columbia (h-index 25, citation count ~4k). Latter is a good point of comparison since he is a bit senior and thus points to a likely path researcher in this category takes. Patrick Schaumont is in a similar (and senior) category. That will define a close peer set for Professor Gerstlauer along with Deming Chen at UIUC and Farinaz Koushanfar.

- *What is your perspective on Professor Gerstlauer's promise for further growth and significant contributions to the field?*

In view of demonstrated efforts by Professor Gerstlauer to reach outside of his background to form new partnerships, the prognosis is good for continued success in attracting students, and raising necessary sponsored research support.

I summary, I find Dr. Gerstlauer's research record strong and worthy of promotion to associate professor with tenure.

If you have any questions, please feel free to contact me.

Sincerely,

Rajesh Gupta, Professor and Chair.

BIOGRAPHICAL SKETCH:

Rajesh K. Gupta is a professor and chair of Computer Science and Engineering at UC San Diego, and holds the QUALCOMM endowed chair. His research interests are in energy efficient systems that have taken turn towards large-scale energy use in recent years. His recent contributions include SystemC modeling and SPARK parallelizing high-level synthesis, both of which are publicly available and have been incorporated into industrial practice. Earlier Gupta lead or co-lead DARPA-sponsored efforts under the Data lntensive Systems (DIS) and Power Aware Computing and Communications (PACC) programs that demonstrated architectural adaptation and compiler optimizations in building high performance and energy efficient system architectures. His ongoing efforts include energy-efficient data-centers and large scale computing using memory-coherent algorithmic accelerators and non-volatile storage systems. ln recent years, Gupta and his students have received a best paper award at lEEE/ACM DCOSS'08 and a best demonstration award at IEEE/ACM lPSN/SPOTS'05. Gupta received a BTech in EE from IIT Kanpur, MS in EECS from UC Berkeley and a PhD in Electrical Engineering from Stanford University. Gupta is a Fellow of the lEEE.

Jilda Gayle

From: Tewfik, Ahmed H <tewfik@austin.utexas.edu>
Sent: Friday, July 19, 2013 5:18 PM
To: Milos Ercegovac; Bearden, Carole A
Cc: Jilda Bolton (jildagayle@gmail.com)
Subject: RE: Letter of reference for Dr. Andreas Gerstlauer

Many thanks Milos!

We greatly appreciate your support.

Regards,
Ahmed

From: Milos Ercegovac [mailto:milos@cs.ucla.edu]
Sent: Friday, July 19, 2013 5:04 PM
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Subject: Re: Letter of reference for Dr. Andreas Gerstlauer
Importance: High

Dear Dr. Tewfik,

Attached is my recommendation letter for the promotion of Prof. Andreas Gerstlauer.
I hope it helps.

Sincerely,

Milos Ercegovac

Short Biography

Prof. Miloš D. Ercegovac
Computer Science Department
University of California at Los Angeles
E-mail: milos@cs.ucla.edu
http://www.cs.ucla.edu/~milos/

Dr. Miloš D. Ercegovac is a Distinguished Professor and a former Chair in the Computer Science Department of the Henry Samueli School of Engineering and Applied Science, University of California at Los Angeles, where he has been on the faculty since 1975. He earned his MS ('72) and PhD ('75) in computer science from the University of Illinois, Urbana-Champaign, and BS in electrical engineering ('65) from the University of Belgrade, Serbia. Dr. Ercegovac has specialized for over 40 years in research and teaching in digital arithmetic, digital and computer system design, and parallel architectures, extensively published in the leading journals and conferences. His dedication to teaching and research has also resulted in several co-authored books: two in the area of digital design (*Digital Systems and Hardware/Firmware Algorithms*, Wiley & Sons, 1985, and *Introduction to Digital Design*, Wiley & Sons, 1999), and two in digital arithmetic (*Division and Square Root: Digit-Recurrence Algorithms and Implementations*, Kluwer Academic Publishers, 1994, and *Digital Arithmetic*, Morgan Kaufmann Publishers - a Division of Elsevier, 2004.) He received the Lockheed-Martin Excellence in Teaching award in 2009. He is also recipient of the 2013 Distinguished Alumni Educator Award from the Department of Computer Science at the University of Illinois at Urbana-Champaign. Dr. Ercegovac has been involved in organizing the IEEE Symposia on Computer Arithmetic since 1978. He served as an associate editor of the IEEE Transactions on Computers 1988 -1992 and as a subject area editor for the Journal of Parallel and Distributed Computing 1986 -1993. Dr. Ercegovac's work has been recognized by his election in 2003 to IEEE Fellow and to Foreign Member of the Serbian Academy of Sciences and Arts in Belgrade, Serbia. He is also a member of the ACM and of the IEEE Computer Society.

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Chair for Embedded Systems

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Prof. Dr. Jörg Henkel

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http://ces.itec.kit.edu/

Jul. 26th, 2013

Reference letter for Dr. Andreas Gerstlauer for promotion to the rank of Associate Professor with tenure

I feel confident to write this reference letter for Dr. Andreas Gerstlauer from University of Texas Austin since I have followed the steps of his career from the time when he was a PhD student at Irvine until now. I also know his research well since I am the Editor-in-Chief of the ACM Transactions on Embedded Computing Systems (ACM TECS) where Dr. Gerstlauer is an Associate Editor. Finally, some of my research is also concerned about system-level design.
In summary, I feel well qualified to write this reference letter and I do not have a conflict of interest since there are no no joint collaborations nor joint publications etc.

Dr. Gerstlauer's research is remarkably broad: He has tackled many highly relevant research topics in the embedded systems field like system-level design methodologies, compilers, OS and even some architectural work.

One of Gerstlauer's core expertise is on system-level design methodologies. Since systems become more and more complex, raising the abstraction level is key in order to efficiently design on-chip systems with billions of transistors. Dr. Gerstlauer was one of the very first to recognize this trend and he has made substantial contributions to the field. He was and is one of the few promoters world-wide to make designers aware of the complexity problem and he is providing solutions in form of design tools and methodologies to cope with the problem.

In the following, I am elaborating on some selected representative work without covering all contributions within this review.
One prominent work that has been led by Dr. Gerstlauer is entitled "Electronic System-Level Synthesis Methodologies" in IEEE Tr. on CAD in 2009. Dr. Gerstlauer and his co-authors make a case for the need for ESL tools (Electronic System Level Design) and claim that many approaches in ESL only cover partial aspects. This is because system level design needs a broad expertise and a broad coverage of methodologies. Facing this problem Dr. Gerstlauer and his co-authors present a novel classification for ESL synthesis tools. They identify current weaknesses of tool flows and present a classification framework for evaluation of different ESL synthesis approaches. This work sheds light into a prominent problem in system-level design and will help to develop tools better suited to today's need of billion-transistor chips.
Another prominent publication of Dr. Gerstlauer is on "Predictive OS Modeling for host-compiled simulation of periodic real-time task sets" in IEEE Embedded Systems Newsletter. This work tackles the problem of host-compiled apprroaches that have been proven to very fast, but at the loss of accuracy. Dr. Gerstlauer and his group present a new methodology based on an OS model that predicts the preemption points by monitoring the system state. One of the key new ideas is that they automatically adjusts the granularity of back-annotated delays. That enables the approach to supersede the then current state-of-the art: Dr. Gerstlauer and his team report 99% of accuracy but at a speedup of more than 200 in average. This is an excellent demonstration of the capabilities of system-level design tools and it shows the leadership Dr. Gerstlauer has in the field. Though there are far more contributions Dr. Gerstlauer has made, but for brevity I choose the two above as representative for his work.
The impact of his research can also be quantified by some numbers: Google Scholar shows 2000+ references to his work and an H-Index of 21 which is excellent given that he is currently at a stage of his career where is considered to be

promoted the rank of Associate Professor with Tenure. Though it is natural that publications of older date dominate the score list of references, it is clearly visible that his research he conducted at UT Austin is clearly picking up and very well received.
Another evidence of excellence is some rewards he received. For instance, a Best Poster Award has been achieved by his student Ardavan Pedram at the International Parallel & Distributed Processing Symposium (IPDPS) Ph.D. forum that is a very prestigious symposium.
Dr. Gerstlauer's work on OS modeling has been selected as one of the most influential contributions in 10 Years at the DATE conference.
It is also remarkable that the initial success he had as a PhD student seamlessly transformed into research success when starting to work independently as an Assistant Professor at UT Austin.

Dr. Gerstlauer has managed to publish at major conferences like ICCAD (IEEE/ACM Intl. Conf on CAD), Codes+ISSS (ESWeek), DATE etc, just to name a few. He has also published in major journals like IEEE Tr. on CAD, IEEE Tr. on Computers (TC). IEEE Tr. on VLSI Systems etc., all are excellent journals is the field.

Dr. Gerstlauer is also very active in services to the community as he is a TPC member and organizer of numerous conferences in the field like DAC, Codes+ISSS, CASES, ASP-DAC, and many more. It is remarkable that he is an Associate Editor of the major journal in embedded system design, namely ACM Tr. on Embedded Computing Systems (this is not yet in his resume as he became an Associate Editor in mid 2013). In summary, he did excellent research community service.

His list of accepted proposals for raising research funds looks very good given the very low acceptance ratios. In several of the projects he is a PI. He has a good mix of NSF, SRC and direct industry funds.

As for his teaching capabilities, I can hardly judge. However, I can indirectly judge since I had the opportunity to listen to some of his talks he gave at conferences. I can state that he is a very good speaker and that he has the capability to explain difficult matters in an easy-to-understand way. When talking to him it became clear that he is a passionate researcher and that he has a deep knowledge of his research field. In addition, he is a very pleasant person to talk to.

As a summary, it is my conviction that Dr. Gerstlauer is a top young researcher. He has shown excellent research capabilities in the past and I believe that he has a great academic research career in front of him. I believe that any EE, CS, ECE department with world rank would be delighted to hire him. I therefore fully support his promotion to the rank of Associate Professor with Tenure.
If there are any further details that need clarification please contact me via email or phone.
Best regards,

(Prof. Jörg Henkel, Karlsruhe Institute of Technology)

About Prof. Jörg Henkel:
He is currently with Karlsruhe Institute of Technology (KIT), Germany, where he is directing the Chair for Embedded Systems CES. Before, he was with NEC Laboratories in Princeton, NJ. His current research is focused on design and architectures for embedded systems with focus on low power and reliability. Prof. Henkel has organized various embedded systems and low power ACM/IEEE conferences/ symposia as General Chair and Program Chair and was a Guest Editor on these topics in various Journals like the IEEE Computer Magazine. He was/is Program Chair of CODES'01, RSP'02, ISLPED/06, SIPS'08 and CASES'09, Estimedia'11, VLSI Design'12, ICCAD'12 and Patmos'13 and served / is serving as General Chair for ICCAD'13, Estimedia 2012, CODES'02, ISLPED 2009. He is/has been a steering committee member of major conferences in the embedded systems field like at ICCAD, ESWeek, ISLPED, Codes+ISSS, CASES and is/has been an editorial board member of various journals like the IEEE TVLSI, IEEE TCAD, JOLPE etc. He has given full/half-day tutorials at leading conferences like DAC, ICCAD, DATE etc and has delivered several keynotes at top international research events.
Prof. Henkel received the 2008 DATE Best Paper Award, the 2009 IEEE/ACM William J. Mc Calla ICCAD Best Paper Award, the Codes+ISSS 2011 Best Paper Award and the MaXentric Technologies AHS 2011 Best Paper Award. He is the Chairman of the IEEE Computer Society, Germany Section, and the Editor-in-Chief of the ACM Transactions on Embedded Computing Systems (ACM TECS). He is an initiator and the coordinator of the German Research Foundation's (DFG) program on 'Dependable Embedded Systems' (SPP 1500) and the site coordinator (of the Karlsruhe site) of the Three-University Collaborative Research Center on Invasive Computing. He is also an elected board member of the German Research Foundation (DFG) on Technical Computer Science. He holds ten US patents.

Jilda Gayle

From: joerg henkel <henkel@ira.uka.de>
Sent: Sunday, July 28, 2013 9:00 AM
To: Bearden, Carole A
Cc: Tewfik, Ahmed H; Jilda Bolton (jildagayle@gmail.com)
Subject: Re: FW: Letter of reference for Dr. Andreas Gerstlauer

Hello,
here is my ref. letter for Andreas Gerstlauer:
https://www.dropbox.com/s/m6gmvtfbc84v5jq/Andreas_Gerstlauer_ref-letter_Jul-2013.pdf
Best regards,
Joerg Henkel

CES - Chair for Embedded Systems
Department of Computer Science
KIT - Karlsruhe Institute of Technology
Building 07.21
Haid-und-Neu-Str. 7
D-76131 Karlsruhe
Germany
http://ces.itec.kit.edu/
Phone: +49 721-608-46050
Fax: +49 721-608-43962

On 7/24/13 10:57 PM, Bearden, Carole A wrote:
> Monday will be fine.
>
> Many thanks,
>
> Carole
>
> -----Original Message-----
> From: joerg henkel [mailto:henkel@ira.uka.de]
> Sent: Wednesday, July 24, 2013 3:51 PM
> To: Bearden, Carole A
> Cc: Tewfik, Ahmed H; Jilda Bolton (jildagayle@gmail.com)
> Subject: Re: FW: Letter of reference for Dr. Andreas Gerstlauer
>
> Dear Prof. Bearden,
> when is the hard deadline? Can I work on this over the weekend so you have it Monday morning?
> Best,
> J. Henkel
>
>
>
> On 7/24/13 8:29 PM, Bearden, Carole A wrote:
>> Dr. Henkel,

Carnegie Mellon

Electrical & Computer ENGINEERING

Pittsburgh, PA 15213-3890
tel: 412.268.4259 • fax: 412.268.1397
jhoe@ece.cmu.edu • www.ece.cmu.edu/~jhoe

James C. Hoe
Professor and Associate Department Head

August 1, 2013

Subject: In support of Prof. Andreas Gerstlauer's Promotion to Associate Professor

Dear Prof. Tewfik:

It is my pleasure to offer this letter in support of Prof. Andreas Gerstlauer's promotion to the rank of Associate Professor with tenure at the Department of Electrical and Computer Engineering at The University of Texas at Austin. I am Professor and Associate Department Head of Electrical and Computer Engineering at Carnegie Mellon University. My main research areas are computer architecture and high-level hardware design and synthesis. More information about me is available at http://www.ece.cmu.edu/~jhoe.

I know Prof. Gerstlauer mainly through his work in Electronic System Level (ESL) design automation and through the conferences we attend. The ESL design automation area grew from several sub-branches of electronics design automations (EDA) that bring high-level—often formal—abstractions and methodologies to address system and chip design tasks (including modeling, simulation, synthesis, verification, evaluation, etc.). This area of research has steadily gained prominence over the last decade in response to the growing scale and prevalence of SoC chip designs. Today, ESL technologies have gained most significant traction in supporting early modeling and simulation of embedded SoC designs, especially in supporting full-fidelity complex software co-development in advance of hardware availability. The scale and cost of chip designs today are at a point that leads me to believe the high-level ESL approaches are at the verge of reaching its full broader impact. As a general comment, at this juncture, it is important that research in this space pay close attention to the coming needs and challenges facing industry practices.

While there are definite similarities in our research interests in ESL and high-level design, I would characterize our approaches as similarly aimed but with Prof. Gerstlauer being more formal and higher-level in abstraction. Prof. Gerstlauer has long been active in ESL research, starting as a PhD student, working and publishing on many problems in the area. Prof. Gerstlauer had made several notable contributions as a graduate student in system-level modeling and simulation related to the SpecC work. He has continued this line of research since joining UT as well as expanding into several areas outside of ESL in collaboration with others. I would say to date, ESL is still not a very large research community, especially in the U.S. Nevertheless, Prof. Gerstlauer has been active and visible in the ESL community and the broader EDA community through his work and

publications; industry and university visits; and organization and technical programming of professional meetings.

I feel Prof. Gerstlauer's accomplishments in the last five years have met the expectation of tenure through a demonstrated trajectory of productivity. (I should explain that I have opinion that five years is a very short time for judging tenure against an absolute benchmark. In computer systems work, there is barely enough time for a PhD student to finish and for a sufficiently bold effort to come to fruition; and that is if nothing went wrong. Therefore, for these shorter tenuring periods, I weigh in my evaluation the amount of activities and the first and second derivatives of trajectory.) The advice I offer often to newly tenured colleagues like Prof. Gerstlauer is to take advantage of their new found station to strategically develop and drive a more strongly themed, many-student flagship effort. Prof. Gerstlauer is working in an area that I view as promising. Prof. Gerstlauer has been successful in raising research funding as PI from many different sources including from competitive NSF programs. He also has a good number of PhD students in the pipeline ready to drive the next stage of his academic career. I look forward to the full realizations of his accomplishments over the coming years.

In closing, I am happy to offer my support for Prof. Gerstlauer's promotion to Associate Professor with tenure in your department. I sincerely hope you would give your most serious considerations to his case. If I can be of any further assistance in this matter, please do not hesitate to contact me.

Sincerely,

James C. Hoe

Jilda Gayle

From: Tewfik, Ahmed H <tewfik@austin.utexas.edu>
Sent: Friday, August 2, 2013 9:37 AM
To: jildagayle@gmail.com
Subject: Fwd: Letter of reference for Dr. Andreas Gerstlauer
Attachments: Gerstlauer_promotion.pdf; Untitled attachment 00062.htm

regards
Ahmed

Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering
The University of Texas at Austin
ENS Room 236
2501 Speedway, C0803
Austin, Texas 78712-0240 USA

Direct: (512) 471-6179
tewfik@austin.utexas.edu

Begin forwarded message:

> **Resent-From:** <[redacted]>
> **From:** "James C. Hoe" <[redacted]>
> **Date:** August 2, 2013, 4:35:19 PM GMT+02:00
> **To:** "'Bearden, Carole A'" <[redacted]>
> **Cc:** "'Tewfik, Ahmed H'" <[redacted]>
> **Subject: RE: Letter of reference for Dr. Andreas Gerstlauer**
>
> Dear Prof. Tewfik,
>
> Please find attached my letter of support
> for Prof. Gerslauer's promotion. Please
> let me know if I can be of any further assistance.
>
> Thanks,
>
> James
>
> -----Original Message-----
> From: Bearden, Carole A [mailto:[redacted]]
> Sent: Wednesday, June 19, 2013 12:46 PM

James C. Hoe

Professor – ECE, CS ; Associate Department Head – ECE ; Co-Director – CALCM, ITRI Lab@CMU

Department	Electrical and Computer Engineering
Office	1113 Hamerschlag Hall
Telephone	(412)-268-4259
Email	jhoe@ece.cmu.edu
Website	http://www.ece.cmu.edu/~jhoe/

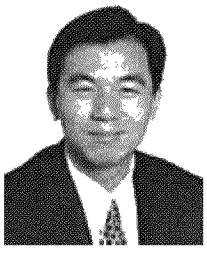
Research Interests

Professor Hoe is interested in many aspects of computer architecture and digital design. His current research areas include:

- Digital Signal Processing Hardware
- FPGA Prototyping and Emulation of Computer Systems
- Pipeline Synthesis from Transaction-based Specifications
- FPGA Architecture for Computing

In the News

- Marculescu, Hoe Named IEEE Fellows
- ECE Celebrates Partnership With Portuguese Business School
- SAFARI/CALCM Paper Published in IEEE Micro's Top Picks
- TRUSS Paper Published in Special Issue of *IEEE Micro*
- Carnegie Mellon Research Team Releases Computer Architecture Simulation Infrastructure
- CSSI Participates in DAC; Hosts Alumni & Friends Reception
- Hoe Wins NSF CAREER Award



Carnegie Mellon, 2000

Research Area

Computer Systems

Keywords

Computer architecture, high-level hardware description and synthesis

Education

PhD, 2000
Electrical Engineering and Computer Science
Massachusetts Institute of Technology

SM, 1994
Electrical Engineering and Computer Science
Massachusetts Institute of Technology

BS, 1992
Electrical Engineering and Computer Science
University of California, Berkeley

Austin, July 20, 2013

Letter of recommendation for the promotion of Dr. Andreas Gerstlauer to the rank of Associate Professor.

Dear members of the evaluation committee,

I am delighted to have the opportunity to recommend Dr. Gerstlauer for tenure at UT Austin. While I had heard of Dr. Gerstlauer's work before, and seen some of his earlier talks, I have interacted with Dr. Gerstlauer much more frequently in about the last three years as some of his more recent work has overlapped strongly with my personal interests and my more recent mission at IBM. I have also recommended his work for funding on a couple of occasions during this period.

I believe that the foundation for our shared interest lies in the fact that Dr. Gerstlauer and I both believe that we need to be willing to optimize across historical boundaries to maintain growth in performance and efficiency of our processing systems in the face of a maturing semiconductor technology. In Dr. Gerstlauer's case, this means stepping beyond the traditional boundary of electronic design automation and taking an interest in architectural and lower-level software considerations. I have followed a similar path, with my earlier work at IBM being more focused on circuits and leveraging technology, and then working on processor architecture, whereas now I try to stretch all the way to systems and middleware optimization.

In general, I would argue that what most impresses me about Dr. Gerstlauer's work, is on the one hand a rigorous drive for the abstraction and elegance one expects of academic research with lasting value, and at the same time a high degree of completeness and realism that allows his research to be readily applicable. It is unusual to see this span of interest and capability within a single researcher.

I have interacted with Dr. Gerstlauer primarily in the context of the work of Ardavan Pedram, the graduate student Dr. Gerstlauer co-advises with Dr. van de Geijn. That said, I have reviewed all five papers submitted as particularly relevant, and I believe I am qualified to comment on them.

The 2009 paper by Gerstlauer e.a. on Electronic System Level Synthesis Methodologies lays the foundation. This paper proposes a classification that emphasizes hardware-software co-design for embedded systems with the double-roof model, and discusses a number of design tools in detail. While this paper was originally aimed at embedded system design, we see this same model emerging now in more general-purpose systems: the very recent addition of hardware-implemented tasks in the OpenCL programming language standard can be seen as matching the approach proposed in this paper. I know that Dr. Gerstlauer already has an interest in the OpenCL framework, and I believe it will provide a context in which his work can extend its reach beyond embedded systems. While OpenCL, though general-purpose and standards-based, is still a language of somewhat limited penetration I foresee that in the not too distant future many of its concepts will find common use in standards such as OpenMP (with OpenMP tasks presenting the equivalent of OpenCL kernels and fit well with the KPN abstraction the paper favors) thus allowing for an even broader relevance of Dr. Gerstlauer's work.

My own work at IBM is focused on increasing the performance of commercial systems by adding reconfigurable (i.e. re-programmable) logic elements to standard commercial servers allowing the practice of hardware-software co-design in a per-application commercial setting. While I have been able to create a number of compelling use cases that will likely justify the addition of such logic to a broad set of server systems, significant advances in design methodology are required to leverage such hardware and increase the efficiency and performance of a broader set of applications. This wil require new design tools and methodologies and thus I am excited about Dr. Gerstlauer's work.

The second paper included for consideration introduces a comprehensive simulation framework. While I cannot pretend to be an expert, I have depended on similar tools in the past, and been close to IBM efforts to develop them. Thus I claim to know enough about the area to recognize that this is high-quality work. In particular, the approach does not abstract away from system aspects that are often ignored because they are not easy to incorporate, but critical to performance, such as operating system and synchronization overheads. The work is applied to sufficiently large examples, and the results, both in terms of simulation performance and accuracy are compelling.

The third paper included for consideration improves on the standard methodology for predicting performance in a preemptive real-time setting by removing the need to select a time-step granularity a priori. The paper explains that errors in the traditional methodology can be significant (and larger than one might expect). The paper convincingly shows that with its adaptive approach timing accuracy vs. simulation performance is significantly enhanced, while removing the need to pick a timing granule relieves the designer from making a difficult choice. Had I been on the program committee for a conference where a paper like this was submitted, I would have recommended it strongly for a best paper award. (This year I have reviewed about 15 conference papers and none were as compelling.)

The fourth paper included for consideration explores allowing some degree of processing error in exchange for lower processing energy. This is a solid contribution, and the paper makes new advances, in particular on how to relate error propagation into (statistical) timing assertions. At the same time of the papers this is the one that due to the combination of algorithm-specific techniques required to arrive at the final result seems more difficult to generalize. Perhaps future work can further build on the notion of a the combination of a computation that allows for the possibility of error followed by a filter. Of course my review is showing a general-purpose bias here … there is nothing intrinsically wrong with research such as this that makes a more specific contribution.

The fifth and final paper submitted for consideration is authored by Ardavan Pedram, who is co-advised by Dr. Gerstlauer and Dr. van de Geijn. I am a member of Ardavan Pedram's Ph.D. committee, and I have met many times with both Ardavan (as well as with Dr. Gerstlauer and Dr. van de Geijn). As evidenced by Ardavan's work Dr. Gerstlauer has instilled in his students the same philosophy that is applied in his earlier work, namely that a rigorous approach will lead to new insights and contributions even in areas that have already received a fair amount of attention, as is the case with leveraging array processors to speed up linear algebra computation. In the case of Ardavan Pedram, the work makes a micro-architectural contribution, but it is the rigorous practice of a true hardware-software co-design exploration where equal attention is being paid to the details and attributes of the implementation of an array processing element, and the hardware-software interactions required to leverage this array processor in an application (via a library), that lifts this work well above the typical contribution in the area. In a typical contribution an interesting micro-architecture may be proposed, but the analysis is usually more superficial and narrow in scope. Discovering the true benefits of what is proposed once realized in a system context is too often left as an exercise to the reader. As an industrial researcher, I am grateful to see work where results are presented that I can truly believe and readily apply.

While I cannot comment directly on Dr. Gerstlauer's performance in the classroom, I have witnessed multiple of his presentations in a number of settings. I have found Dr. Gerstlauer to be an effective and engaging presenter, and thus would find it hard to believe if his effectiveness as a teacher was anything less than outstanding.

In summary, **I strongly recommend extending tenure and the associate professor rank to Dr. Gerstlauer**. I believe that his work is of exceptional quality and rigor, and the type of work that those of us who have to bridge between academia and commercial practice look for. Dr. Gerstlauer achieves this rigor and detail without sacrificing his quest for the fundamentals of elegance and abstraction, thus allowing his work to be simultaneously of academic and practical importance. I also believe that hardware-software co-design will be a field of further growing importance, as in the future we will have to practice this approach even in computer systems we consider general-purpose. Because I work on general purpose server systems that include reconfigurable logic, Dr. Gerstlauers work is directly relevant to me. As evidenced by the quality of the work of his graduate students and the effectiveness of his presentations, Dr. Gerstlauer is also an outstanding educator and mentor.

Please do not hesitate to contact me if there are any further questions.

Sincerely,

H. Peter Hofstee, Ph.D.
IBM Austin Research Laboratory
11501 Burnett Rd.
Austin, TX, 78703
+1 512 284 3193

Jilda Gayle

From: Peter Hofstee <hofstee@us.ibm.com>
Sent: Tuesday, July 23, 2013 9:01 PM
To: Bearden, Carole A
Cc: Jilda Bolton (jildagayle@gmail.com); Tewfik, Ahmed H
Subject: Re: Letter of reference for Dr. Andreas Gerstlauer
Attachments: Gerstlauer Letter Hofstee Signed.pdf; CV_2010_Non_Confidential_B.pdf

Hello Carole,

Here is the signed copy of the letter I sent earlier (no other changes), and also a copy of my resume.
The latter is about 3 years old (but up-to-date as to my current job). Do let me know if that is an issue.

(See attached file: Gerstlauer Letter Hofstee Signed.pdf)(See attached file: CV_2010_Non_Confidential_B.pdf)

Best regards, -Peter

H. Peter Hofstee
IBM Austin Research Laboratory
11500 Burnet Rd
Austin, TX 78758
Cell 512 284 3193

"Bearden, Carole A" ---07/03/2013 10:28:37 AM---Dr. Hofstee, Thank you for your support of Dr. Andreas Gerstlauer promotion and agreeing to write a

From: "Bearden, Carole A" <cjjp@mail.utexas.edu>
To: Peter Hofstee/Austin/IBM@IBMUS,
Cc: "Tewfik, Ahmed H" <tewfik@austin.utexas.edu>, "Jilda Bolton (jildagayle@gmail.com)" <jildagayle@gmail.com>
Date: 07/03/2013 10:28 AM
Subject: Letter of reference for Dr. Andreas Gerstlauer

Dr. Hofstee,

Thank you for your support of Dr. Andreas Gerstlauer promotion and agreeing to write a recommendation letter. Attached is a formal request for the letter with a website, logon and password to access his information as well as his CV.

Best regards,

Carole Bearden
Executive Assistant
The University of Texas at Austin
Electrical and Computer Engineering
ENS Room 236
2501 Speedway, C0803
Austin, Texas 78712-0240 USA

[attachment "Gerstlauer-Hofstee.pdf" deleted by Peter Hofstee/Austin/IBM] [attachment "Andreas Gerstlauer-Resume.pdf" deleted by Peter Hofstee/Austin/IBM]

CURRICULUM VITAE

Name & address:

Harm Peter Hofstee
704 Pressler St., Austin, TX 78703, USA

Present Position:

Senior Technical Staff Member
Workload-Optimized and Hybrid Systems
IBM Austin Research Laboratory
July 2010 -

Previous Positions

Distinguished Engineer, Cell/B.E. Chief Scientist
IBM Systems and Technology Group
2006 - July 2010

Senior Technical Staff Member (full time), Cell SPE Chief Architect
IBM Microelectronics Division / IBM Systems and Technology Group
May 2001 - 2006

Research Staff Member (full time)
IBM Austin Research Laboratory
Aug 1996 - April 2001

Lecturer (Member of the Faculty, full time)
California Institute of Technology, Computer Science Department
Oct 1994 - June 1996

Teaching Assistant / Research Assistant (20hrs/wk)
California Institute of Technology, Computer Science Department
Oct 1989 - Sep 1994

Teaching Assistant / Research Assistant (full time)
Groningen University, Netherlands, Computer Science Department
Oct. 1988 - Aug. 1989

Army Officer (Draft, final rank 2nd Ltn., full time)
Netherlands Army
Mar. 1987 - July 1988

Student Assistant (8 hrs/wk)
Groningen University, Netherlands, Computer Science Department
Sep. 1984-Aug 1985

Degrees:

Ph.D., Computer Science, California Institute of Technology, 1995 (completed Sept. 1994)
Thesis title: Synchronizing Processes

M.S., Computer Science, California Institute of Technology, 1991

Thesis title: Constructing Some Distributed Programs

Drs., Theoretical Physics, Rijks Universiteit Groningen, The Netherlands, 1988
Thesis title: Superspace Perturbation Theory

A SUMMARY STATEMENT OF MY RESEARCH CAREER:
(Please do note that for the last 10 years I have worked in processor development, not research.)

Major Research Accomplishments and Current Work:

* I made significant contributions to the architecture and definition of the "Cell" project, a collaboration between Sony, Toshiba and IBM. I was chief architect of the Synergistic Processor Element that provides the bulk of the computational power and the foundation for security in the Cell processor. The Cell Broadband Engine and its derivatives including the PowerXCell processor are used in a wide variety of systems including the Sony Playstation3, the IBM QS20/21/22 servers and the "Roadrunner" petaflop supercomputer at Los Alamos National Laboratory. I have published widely on this work and given numerous presentations at major international conferences.

* I have participated in multiple pre-product processor design programs with IBM server group. Except for some patents this work remains confidential and unpublished.

* I have given multiple conference presentations and written multiple papers on power effciency metrics and computer architecture to improve for power efficiency. Power dissipation is the major limiter of microprocessor performance in the foreseeable future.

* At IBM Austin I was responsible for chip logic design, coordination, and testing for the world's first 1GHz CMOS microprocessor, containing about 1 million transistors.

* I played a leading role in a follow-on, more complete, version of the 1GHz microprocessor, containing 19 million transistors. This processor was built in relatively old technology, but on a technology-invariant basis (cycle time measured in inverter delays) this processor is the fastest processor that has ever been built. This processor design proves that in the future additional frequency growth in products can be obtained by a combination of high-frequency dynamic circuits, an extremely disciplined logic design, and careful floorplanning. To get an equivalent improvement from semiconductor technology alone would require at least two CMOS generations, each costing about a billion dollars to develop. I presented the results at the '2000 International Solid State Circuits Conference, the premier forum in the world for this kind of work.

* While at Caltech I designed several asynchronous quasi delay-insensitive circuits. Five of my designs (caches, memories and register files) were fabricated, and all were found to be fully functional. To my knowledge, these asynchronous memories were the first of their kind.

* As a part of my PhD research at Caltech I constructed a theory for the refinement of concurrent programs. Whereas traditionally the verification of these programs requires one to consider a number of cases that is proportional to all possible interleavings of the processes (this number of cases soon becomes intractable), I showed that under certain conditions only a single interleaving, consistent with the original more sequential program, needs to be considered. For most concurrent programs, specifically for those that describe microprocessors, the conditions can usually be easily shown to hold.

* To test the theories of my PhD research in practice I had a class of about 30 students each refine an interpreter for a meaningful subset of Java byte codes into a program describing an innovative superscalar out of order processor, a process that typically requires several engineers to spend several years.

* While at the University of Groningen in the Netherlands in 1988/89, and later at the California Institute of Technology (Caltech) I studied the construction and correctness of concurrent programs. I solved a long standing problem to formally construct a distributed sorting program using message passing, and later extended the algorithm to an algorithm for sorting, and a similar one for load balancing, on arbitrary networks of computers. These later algorithms are amongst the most complex concurrent algorithms proven to be correct.

Carnegie Mellon

Electrical & Computer ENGINEERING

Pittsburgh, PA 15213-3890
ph: 412.268-3545 • fax: 412.268-1374
thomas@ece.cmu.edu • www.ece.cmu.edu

Don Thomas
Professor

July 26, 2013

Dr. Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering
The University of Texas at Austin

Dear Dr. Tewfik:

I am writing to express my enthusiastic support for the promotion of Dr. Andreas Gerstlauer to Associate Professor with Tenure in your department. I have known Andreas for about 7-8 years, mainly through seeing his presentations at conferences and through joint service on conference program committees.

Andreas is well known for his research work in system level design automation methodologies. He is successfully following on from his thesis and post-doc research in the area of simulation, synthesis and compilation of designs from system level models. I was pleased to see that his paper "RTOS Modeling for System Level Design" published in 2003 was recently listed in the most influential papers in ten years of the Design Automation and Test Europe (DATE) conference. DATE is widely respected and deeply technical conference in our field. The paper proposed a model of real-time operating systems based on features currently available in system level design languages. At the time, several research groups were searching for a means to bring the hardware and software models of these systems together. This work did just that and enabled higher level modeling of these systems that, in turn, can make designers more efficient.

I have recently read some of his later papers or heard some of his presentations on his "host-compiled" modeling of embedded systems. This is a back annotation technique that enables source code intended for execution in a target system to be annotated with timing and power metrics. As simulation proceeds, the annotations provide measures of the system execution to the simulation kernel. This approach has been able to attain high speeds and great accuracy; important issues in the simulation community for these large systems. This is important work for the embedded system design methodology community and I see its success as a direct result of his leadership. Although his Ph.D. advisor, Professor Dan Gajski, is well known in this field, Andreas has clearly taken steps beyond his initial work with him.

I haven't followed him closely in some of his other research areas so I'll rely on others to comment on those.

Andreas' research presentations are very well done. They are engaging and I've seen him answer questions with great clarity and providing deeper insight. I assume that his presentation capability carries over into his classroom as it appears that he gets good ratings for his teaching.

I observe that he has published 9 journal papers and 35 refereed conference proceedings papers since his work with his advisor. Some of the conferences he publishes at have very high standards. From my knowledge these include: ICCAD, DATE, DAC, ASP-DAC, and

CODES+ISSS. These conferences are known for their blind reviews of complete manuscripts and their low acceptance ratios. In a fast moving technical field, these are considered nearly at the level of a journal.

In summary, I think that Andreas is a rising star. He has come out of the research group of a prominent thesis advisor and has established himself as a strong technical leader in the computer system design methodology field. His research group's software is being used and is influencing other research. I enthusiastically endorse his promotion to Associate Professor with tenure.

Sincerely,

Donald E. Thomas
Professor of Electrical and Computer Engineering
Carnegie Mellon University

Jilda Gayle

From: Tewfik, Ahmed H <tewfik@austin.utexas.edu>
Sent: Friday, July 26, 2013 2:55 PM
To: jildagayle@gmail.com
Subject: FW: recommendation letter for Andreas Gerstlauer
Attachments: AndreasGerstlauer.pdf; ATT00001.htm
Signed By: tewfik@austin.utexas.edu

Regards,
Ahmed

From: Don Thomas [mailto:thomas@ece.cmu.edu]
Sent: Friday, July 26, 2013 1:57 PM
To: Tewfik, Ahmed H
Cc: Bearden, Carole A
Subject: Re: recommendation letter for Andreas Gerstlauer

Professor Tewfik,
attached please find my promotion letter regarding Andreas.
Sincerely,
-Don Thomas

Donald E. Thomas received the Ph.D. degree in 1977 from the Carnegie Mellon University where he is currently Professor of Electrical and Computer Engineering, working in the areas of single-chip heterogeneous multiprocessor systems, FPGA acceleration of computational tasks, and chip architecture design for yield improvement and lifetime reliability. He is co-author of the book "The Verilog Hardware Description Language" which through five editions has also been translated into Japanese and Mandarin Chinese. From 1985 to 1986 he was a Visiting Scientist at IBM T.J. Watson Research Center, Yorktown Heights, NY. He was chair of the 1989 Design Automation Conference. He has been on the editorial board of IEEE Design and Test Magazine, an Associate Editor for the IEEE Transactions on VLSI Systems and ACM's Transactions on Embedded Systems, and on the IEEE Computer Society Board of Governors. He has been chair of the CODES/CASHE-96 Workshop on Hardware/Software Co-design and is now Steering Committee Chair for Embedded Systems Week (ESWeek). He was elected Fellow of the IEEE "For contributions to automatic design of integrated circuits and systems, and to education in computer engineering." He was elected Fellow of the ACM "In recognition of outstanding technical and professional achievements in the field of information technology"

Donald E. Thomas

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Jilda Gayle

From: Bearden, Carole A <cjjp@mail.utexas.edu>
Sent: Monday, August 19, 2013 3:17 PM
To: Jilda Bolton (jildagayle@gmail.com)
Subject: FW: letter for Andreas Gerstlauer

-----Original Message-----
From: Wolf,Marilyn Claire [mailto:marilyn.wolf@ece.gatech.edu]
Sent: Friday, July 26, 2013 7:42 AM
To: Bearden, Carole A
Cc: Marilyn Wolf
Subject: letter for Andreas Gerstlauer

I am writing to give my highest recommendation to Dr. Andreas Gerstlauer for promotion to Associate Professor. I have known Andreas since he was a graduate student thanks to our mutual interest in embedded computing.

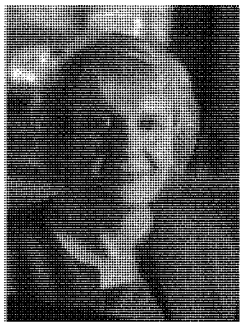
Dr. Gerstlauer is internationally recognized for his work in system-level modeling and synthesis. A key to system-level synthesis is modeling of performance and energy. Dr. Gerstlauer has developed important new methods for modeling processors and operating systems that combine simulation and prediction. He has also worked for many years in system synthesis, starting with his work in SpecC. He has also applied these techniques to important domains, including multimedia and numerical methods. I am revising my book High-Performance Embedded Computing and have cited several of Dr. Gerstlauer's papers on these topics in my revision.

Dr. Gerstlauer has an outstanding record of publication. He has published in very prestigious journals including IEEE Transactions on Computers, IEEE Transactions on VLSI Systems, and IEEE Transactions on CAD. He has published extensively in the major conferences in embedded computing. He has an outstanding record of funding from multiple sources, including government and industry. He has a strong record of producing Ph.D. students. He has a very strong record of service to the research community; I have worked with him on conferences.

Overall, I think that Dr. Gerstlauer is an extremely strong candidate for promotion based on his widely recognized stature in embedded computing. I give him my highest recommendation. Please feel free to contact me if you have any questions.

--
Marilyn Wolf
marilyn.wolf@ece.gatech.edu
School of ECE, Georgia Institute of Technology
777 Atlantic Drive NW, Atlanta GA 30332
voice: 404 894 5933 fax: 404 3485 1746
http://www.ece.gatech.edu/research/labs/esl/wolf.html
Book Web site: http://www.marilynwolf.us Read my food blog: http://foodwolfblog.blogspot.com/ My photos:
http://www.marilynwolf.us/Photography/

Faculty Profile - Marilyn C Wolf



Professor; Rhesa "Ray" S. Farmer, Jr., Distinguished Chair in Embedded Computing Systems; Georgia Research Alliance Eminent Scholar
VLSI Systems and Digital Design

Phone: 404.894.5933
Fax: 404.385.1746
Office: Klaus 2352A
Email GT Directory Entry
http://www.ece.gatech.edu/research/labs/esl/wolf.html

Biography

Marilyn Wolf received her bachelor's, master's, and doctoral degrees in electrical engineering from Stanford University in 1980, 1981, and 1984, respectively. She was with AT&T Bell Laboratories in Murray Hill, N.J. from 1984 to 1989 and was with Princeton University from 1989 until 2007. In July 2007, Dr. Wolf joined Georgia Tech as the Rhesa "Ray" S. Farmer, Jr. Distinguished Chair in Embedded Computing Systems and Georgia Research Alliance Eminent Scholar. She has developed a number of techniques for embedded computing, ranging from hardware/software co-design algorithms and real-time scheduling algorithms to code compression and distributed smart cameras. She is a co-founder of Verificon Corporation, which designs smart camera systems. She helped to start several technical conferences, including CODES and MPSoC. She has written four textbooks.

Selected Publications, Patents

Research Interests

- Embedded computing architectures
- Software for embedded computing
- Methodologies and tools for embedded computing system design
- Smart cameras and smart microphones
- VLSI systems
- Biochips

Distinctions

- IEEE Circuits and Systems Society Education Award, 2006
- ASEE Frederick E. Terman Award, 2003
- IEEE Computer Society Golden Core Award
- Fellow, IEEE and ACM (Association for Computing Machinery)

UNIVERSITY OF ILLINOIS
AT URBANA-CHAMPAIGN

College of Engineering
Office of the Dean
306 Engineering Hall, MC-266
1308 West Green Street
Urbana, IL 61801

August 19, 2013

Dear Professor Tewfik,

I am writing this letter in support of Prof. Andreas Gerstlauer's promotion to Associate Professor with tenure. Andreas has an outstanding research, teaching and service record, and we would be glad to have him on our faculty here at UIUC. I strongly support his promotion.

Andreas has made significant contributions to the broader field and to his specific area of system-level design automation. With embedded systems and systems-on-chip (SoCs) driving innovations in many areas, such as mobile computing, transportation or health care, complexities of corresponding devices continue to grow exponentially and there is a continued need for new electronic design automation methods to enable us to develop the systems of the future. One way to manage complexities is to raise the level of abstraction in design, but this requires new concepts, methods and tools to be developed from the ground up. Andreas' work has helped lay the foundations for establishing such new design automation solutions at higher levels of abstraction, namely the system level. At the same time, he has recently branched out to bring his system-level expertise into addressing some of the fundamental technological challenges that we are facing in the design of future computer systems, with energy efficiency being one of the primary concerns there.

Dating back to results coming out of his Ph.D. and post-doctoral work, Andreas is a core member of the group developing the SpecC system-level design language (SLDL) and design methodology, where he was originally instrumental in shaping language definitions and, more importantly, development of a rigorous design methodology and system modeling solutions on top of basic language concepts. Before this, the field of system-level design was really in its infancy. As such, results of this work have achieved far-reaching recognition in both academia and industry. Specifically, research on language and modeling concepts that Andreas was deeply involved with have heavily influenced development of the SystemC language and so-called transaction-level modeling (TLM) approaches around it, both of which have been standardized by IEEE and are widely used in industry today. Andreas also led the development of the SpecC-based System-on-Chip (SCE) framework and tool set, which was one of the first complete system-level design automation solutions, and which he helped bring into a commercial and industrial setting in a collaboration with the Japanese Aerospace Exploration Agency (JAXA) that was established under his lead. Since joining UT Austin, he has continued to make significant contributions in the area of system modeling and system-level design, and he is widely recognized as one of the experts in the field, as evidenced by several widely cited books and position/survey papers he has published over the years.

Since joining UT Austin, Andreas has established a diverse and high-quality research program that is certainly on par with if not better than any of his peers'. When compared within the field, Andreas' has high funding level from a range of diverse sources. This includes fundamental and competitive long-/medium-term grants and contracts from relevant federal agencies and industry consortia, such as the Semiconductor Research Corporation (SRC). Having received several SRC grants over the years myself, I can attest to their competitiveness, which is certainly equal to that of NSF proposals. In our area, SRC grants are highly desired, because they demonstrate industry relevance and provide a path to impacting industrial practice. With federal budgets continuing to decline, it is particularly noteworthy that Andreas has established strong industry contacts that have also allowed him to secure funding from individual industry sources directly. Furthermore, Andreas has over and over demonstrated the desire to not stop at producing only papers, but to also release working prototypes that bring technology to a point where it can be transferred into practice and thus eventually have an impact on real-world problems, which is highly commendable.

telephone 217-333-2150 • *fax* 217-244-7705

For these reasons, Andreas is highly visible, well known and respected in the broader design automation community. This is evidenced by several prestigious service appointments he currently holds or has held. Andreas has been part of the Technical Program Committee of all the major conferences in the field, and especially the ones most relevant to his specific area, such as CODES+ISSSS. In addition, he has in many cases served as Track Chair, he serves as Associate Editor for the main journal in his area (ACM Transactions on Embedded Computer Systems – IEEE does not have a journal in his specific area), and he is currently Chair of the System-Level Design Track of the Design Automation Conference (DAC), which is *the* premier conference bringing together the design automation community. This is a significant honor and a high-profile position.

Andreas also has a strong teaching record. I have personally observed him give talks in (special) sessions at conferences, and as such, I have seen his ability to succinctly and concisely present concepts first hand. At UT Austin, I was particularly impressed by the graduate class on System-on-Chip Design that he has developed there. It uniquely combines theoretical aspects about electronic system-level synthesis with practical labs and a project that immerse students in an industrial-strength design flow using industry-standard tools. This provides an excellent foundation for training future generation of engineers. I am also aware that he has regularly offered this same class not only in the regular graduate program, but also in a professional master's program that provides continuing education for students with full-time jobs in industry. Furthermore, at the introductory undergraduate level, I have seen that he is involved in an effort at UT Austin to develop a Massively Open Online Course (MOOC) on embedded system design. All of these demonstrate Andreas' passion as an educator to impart knowledge in crucial technological areas to a broad audience.

In summary, I highly recommend Andreas for the promotion to tenured Associate Professor at ECE of UT-Austin.

Sincerely,

Martin D. F. Wong
Edward C. Jordan Professor of Electrical and Computer Engineering
Acting Associate Dean for Academic Affairs

telephone 217-333-6057 • fax 217-244-7705

Jilda Gayle

From: Wong, Martin D F <mdfwong@illinois.edu>
Sent: Monday, August 19, 2013 5:35 PM
To: Tewfik, Ahmed H
Cc: Jilda Bolton (jildagayle@gmail.com); Bearden, Carole A
Subject: RE: URGENT - Letter of reference for Dr. Andreas Gerstlauer
Attachments: gerstlauer13.pdf

Importance: High

Dear Prof. Tewfik,

Please see attached reference letter for Prof. Gerstlauer's promotion case. Sorry for sending the letter late.

Thanks.

-Martin

From: Bearden, Carole A [mailto:cjjp@mail.utexas.edu]
Sent: Tuesday, August 13, 2013 11:46 AM
To: Wong, Martin D F
Cc: Tewfik, Ahmed H; Jilda Bolton (jildagayle@gmail.com)
Subject: URGENT - Letter of reference for Dr. Andreas Gerstlauer
Importance: High

Dr. Wong,

Per our phone conversation the new deadline for your recommendation letter for Dr. Gerstlauer will be August 16th.

Thank you so much.

Best regards,

Carole

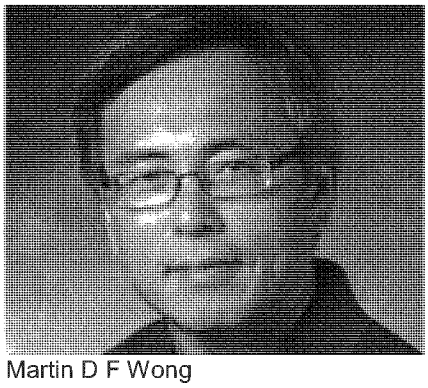
From: Bearden, Carole A
Sent: Monday, August 05, 2013 4:31 PM
To: [redacted]
Cc: Tewfik, Ahmed H ([redacted]); Jilda Bolton ([redacted])
Subject: URGENT - Letter of reference for Dr. Andreas Gerstlauer
Importance: High

Dr. Wong,

This is a gentle reminder that your recommendation letter for Dr. Gerstlauer was due July 20th. Please let me know if you need further information.

Many thanks,

MARTIN D F WONG



Martin D F Wong
Professor
409 Coordinated Science Lab, MC 228
1308 W. Main St.
Urbana, Illinois 61801
217-244-1729
mdfwong@illinois.edu

Primary Research Area

- Circuits - Computer aided design of integrated circuits

Profile Sections

- Overview
- Research
- Honors

Education

Ph.D. in Computer Science, University of Illinois at Urbana-Champaign, January 1987

Research Interests

- Combinatorial optimization
- Design and analysis of algorithms
- Field-programmable systems
- Design for Manufacturing
- CAD for VLSI Electronic Packaging
- Computer-aided design of VLSI

Research Areas

- Algorithms and computational complexity
- Circuits
- Circuits
- Computer aided design of integrated circuits
- Logic design and VLSI

Honors, Recognition, and Outstanding Achievements for Research

- Canadian National Descartes Mathematics Competition, 1st Place (Toronto) and 4th Place (National), 1975.
- Hans Heillbronn Prize in Pure Mathematics, University of Toronto, 1978.
- Undergraduate Scholarships: i) William Hossack Memorial Scholarship, ii) Samuel Beatty Scholarship, and iii) Burton Scholarship, University of Toronto, 1977-1979.

- University Fellowship, University of Illinois at Urbana-Champaign, 1979-1980 and 1981-1982.
- Best Paper Award, 23rd ACM/IEEE Design Automation Conference (DAC), 1986.
- Best Paper Award Nomination - ACM/IEEE Design Automation Conference (DAC), 1990.
- IBM Faculty Development Award, 1989-1991.
- National Science Foundation Research Initiation Award, 1989-1992.
- ACM/IEEE Design Automation Fellowship, 1991 and 1994.
- Best Paper Award, IEEE International Conference on Computer Design (ICCD), 1995.
- Best Paper Award Nomination - IEEE Transactions on Computer-Aided Design (TCAD), 1998.
- Endowed Faculty Fellow in Computer Sciences, University of Texas at Austin, 1990-1999.
- Best Paper Award Nomination - IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 1999.
- ACM Recognition of Service Award, 1999.
- Best Paper Award Nomination - IEEE Transactions on Computer-Aided Design (TCAD), 1999.
- IBM Faculty Partnership Award, 2000.
- 2000 CAD Transactions Best Paper Award. (Given to the best paper chosen from all papers published in IEEE Transactions on Computer-Aided Design in 1998 and 1999.)(This has been renamed as the Donald O. Peterson Best Paper Award.), 2000.
- Best Paper Award Nomination - IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2001.
- David Bruton Centennial Professorship in Computer Sciences, University of Texas at Austin, 2001-2002.
- Best-of-20-Years ICCAD Paper. (Our ICCAD-94 paper on circuit partitioning was among one of the 42 papers, out of all ICCAD papers in 1983-2002, chosen to be included in the book, The Best of ICCAD - - 20 Years of Excellence in Computer Aided Design, published by ICCAD in its 20th anniversary in 2002.), 2002.
- Best Paper Award Nomination, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2004.
- IBM Faculty Award, 2004.
- Best Paper Award Nomination, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2005.
- Best Paper Award Nomination, IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2005.
- IEEE Distinguished Lecturer, Circuits and Systems Society, 2005-2006.
- Best Paper Award Nomination, IEEE International Symposium on Quality Electronic Design (ISQED), 2008.
- Fellow, IEEE

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